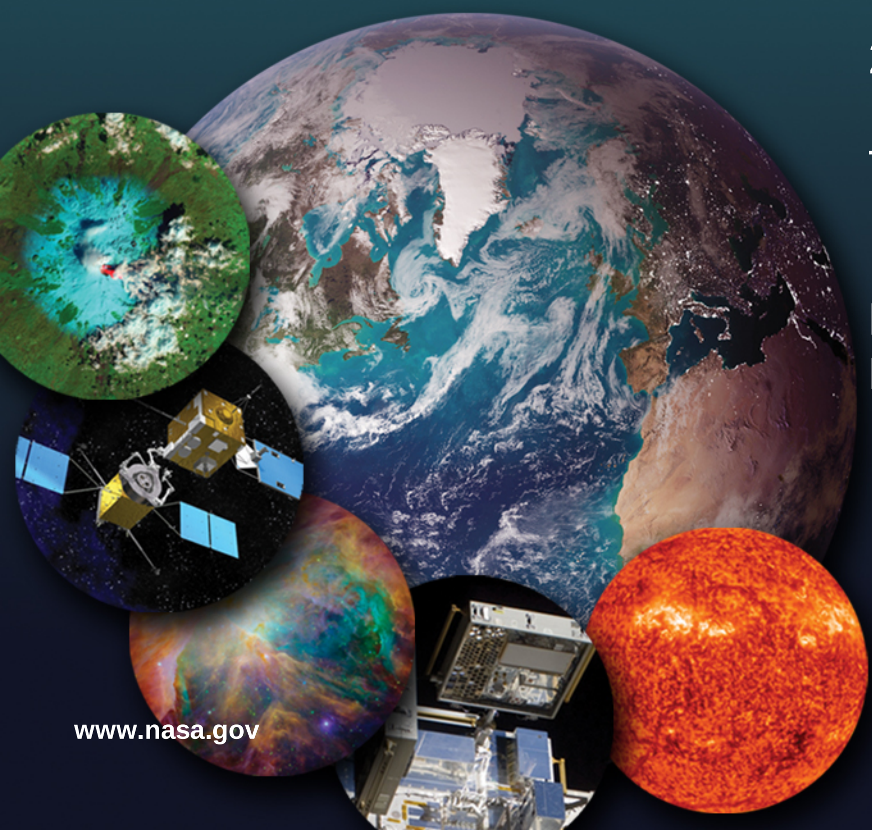
National Aeronautics and Space Administration

Adapting the Reconfigurable SpaceCube Processing System for Multiple Mission Applications



2014 IEEE Aerospace Conference

Track 7.05: Reconfigurable Computing Systems Technologies

Dave Petrick
Embedded Systems Group Leader

SpaceCube

SCIENCE DATA PROCESSING BRANCH
Code 587 • NASA GSFC

SpaceCube, Target Applications

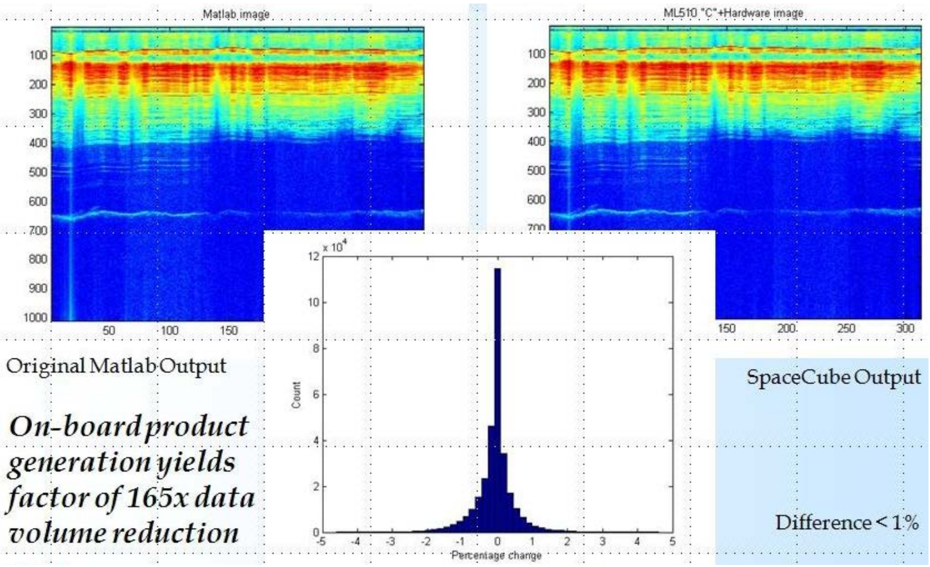
- Small, light-weight, reconfigurable multi-processor platform for space flight applications demanding extreme processing capabilities
  - Reconfigurable Components: FPGA, Software, Mechanical
  - Promote reuse between applications
- Hybrid Flight Computing: hardware acceleration of algorithms to enable onboard data processing and increased mission capabilities

Hardware Algorithm Acceleration

Application	Xilinx Device	Acceleration vs CPU
SAR Altimeter	Virtex-4 FX60	**79x** vs PowerPC 405 (250MHz, 300 MIPS)
RNS GNFIR FPU, Edge	Virtex-4 FX60	**25x** vs PowerPC 405 (250MHz, 300 MIPS)
HHT EMD, Spline	Virtex-1 2000	**3x** vs Xeon Dual-Core (2.4GHz, 3000 MIPS)
Hyperspectral Data Compression	Virtex-1 1000	**2x** vs Xeon Dual-Core (2.4GHz, 3000 MIPS)
GOES-8 GndSys Sun correction	Virtex-1 300E	**6x** vs Xeon Dual-Core (2.4GHz, 3000 MIPS)

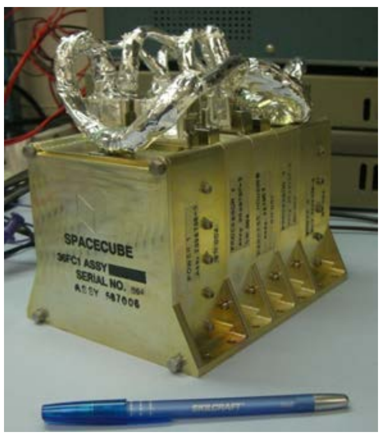
<u>Notes</u>:
1) **All functions involve processing large data sets (1MB+)**
2) **All timing includes moving data to/from FPGA**
3) **SpaceCube 2.0 is 4x to 20x more capable than these earlier systems**

On-Board Data Reduction



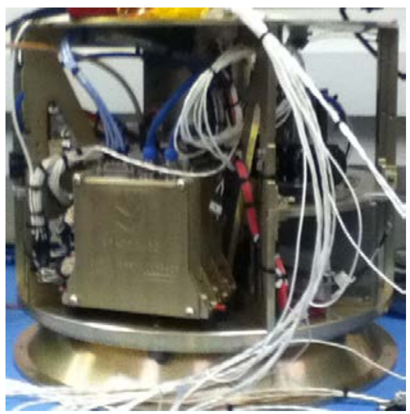
SpaceCube Family Overview

v1.0



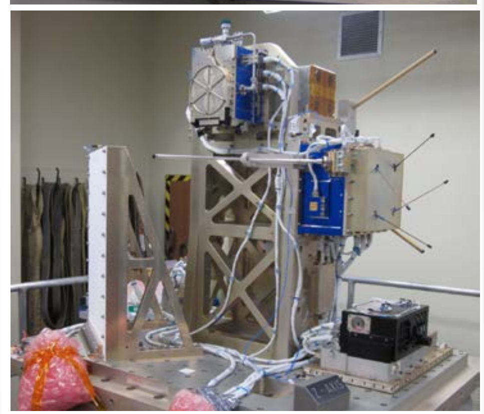
2009 STS-125
2009 MISSE-7
2013 STP-H4
2015 STP-H5

v1.5



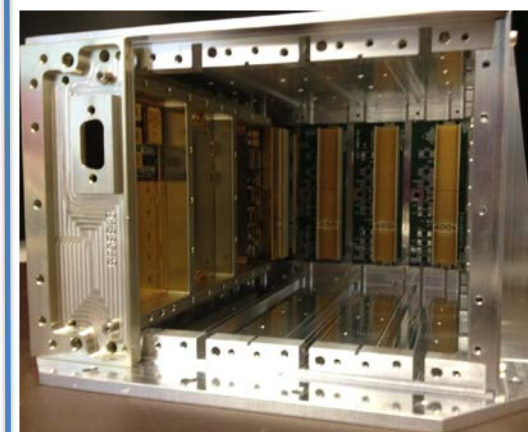
2012 SMART

v2.0-EM



2013 STP-H4
2015 STP-H5

v2.0-FLT



2015 GPS Demo
- Robotic Servicing
- Numerous proposals for Earth/Space/Helio

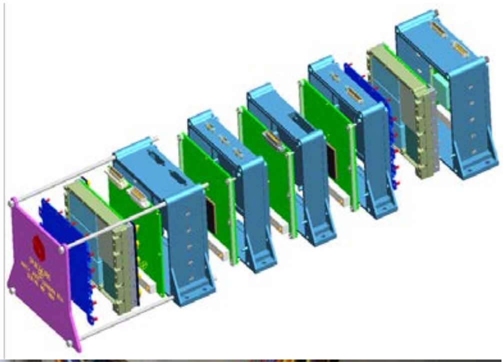
High Performance Space Processing

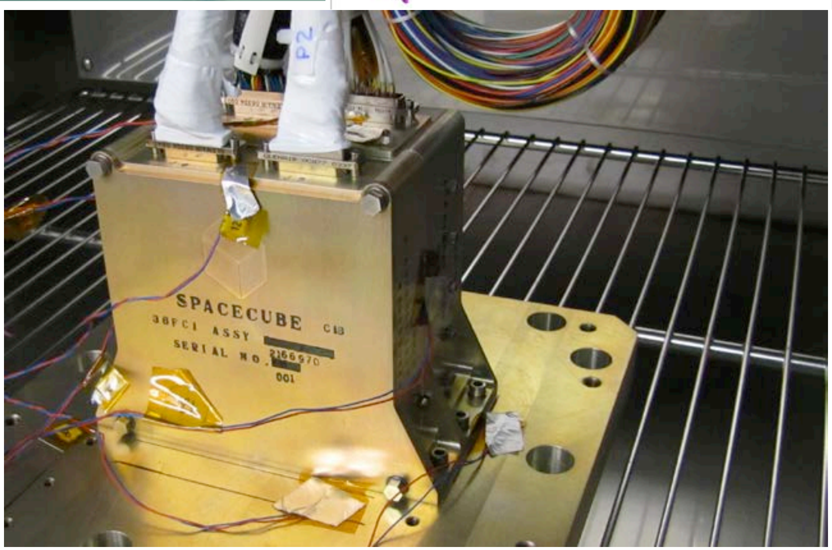
- Challenge
  - Need order of magnitude performance improvement over traditional space processors
  - Unlock mission enabling technology
  - Keep size and power under control
- Approach
  - Rad-Hard processor will not work, generations behind, large
  - Science data doesn’t have to be perfect 100% of the time
  - MIPS/Watt metric
- Our Solution
  - Hybrid processing using FPGA, CPU, DSP computing nodes
  - Hardware accelerated computing
  - System monitor, critical controller

SpaceCube: a high performance reconfigurable science data processor based on Xilinx Virtex FPGAs

SpaceCube v1.0 System

Mechanical Slice Stacking Architecture





Base Unit Size: 4.5” x 4.3” x 3”
Operating Range: -30C to +55C
Power: 12-16W

Processor Slice, Back-to-Back Architecture

FPGAs: 2x Xilinx V4FX60, 2x Aeroflex UT6325
Memory: 1GB SDRAM, 1GB NAND Flash, PROM/SRAM
External I/O: 20ch LVDS/RS422

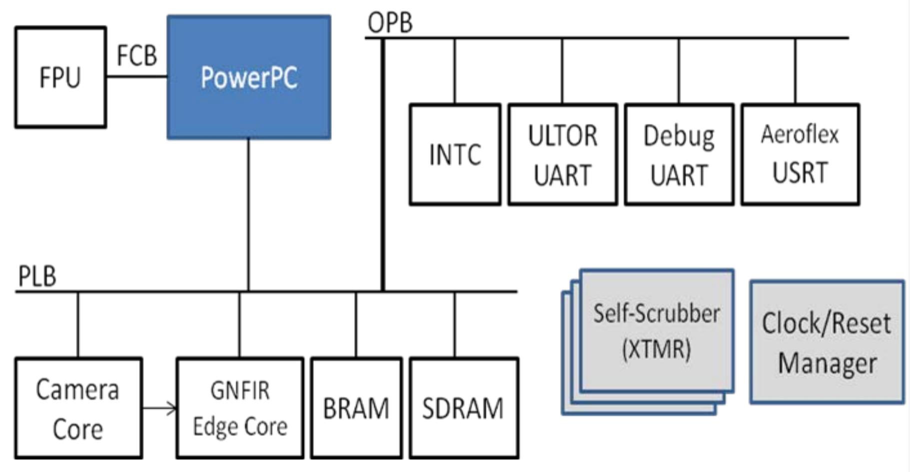
Power Slice, Two Cards

28V Input, 5V, 3.3V, 2.5V, 1.5V, +/-12V Outputs
External I/O: 1553, 10Base-T Ethernet, 4ch RS422

SpaceCube v1.0 Missions

Year	Mission	Application
5/2009	Relative Navigation Sensors STS-125	Real-time image processing/tracking, data compression, shuttle interface
11/2009-Present	MISSE7/8	Radiation Experiment
2010-2011	Argon Robotic Ground Demo	Similar to RNS with additional instruments, upgraded algorithms
8/2013-Present	STP-H4, DoD Delivery	Payload Control, ISS Interface
2015	STP-H5, DoD Delivery	Payload Control, ISS Interface

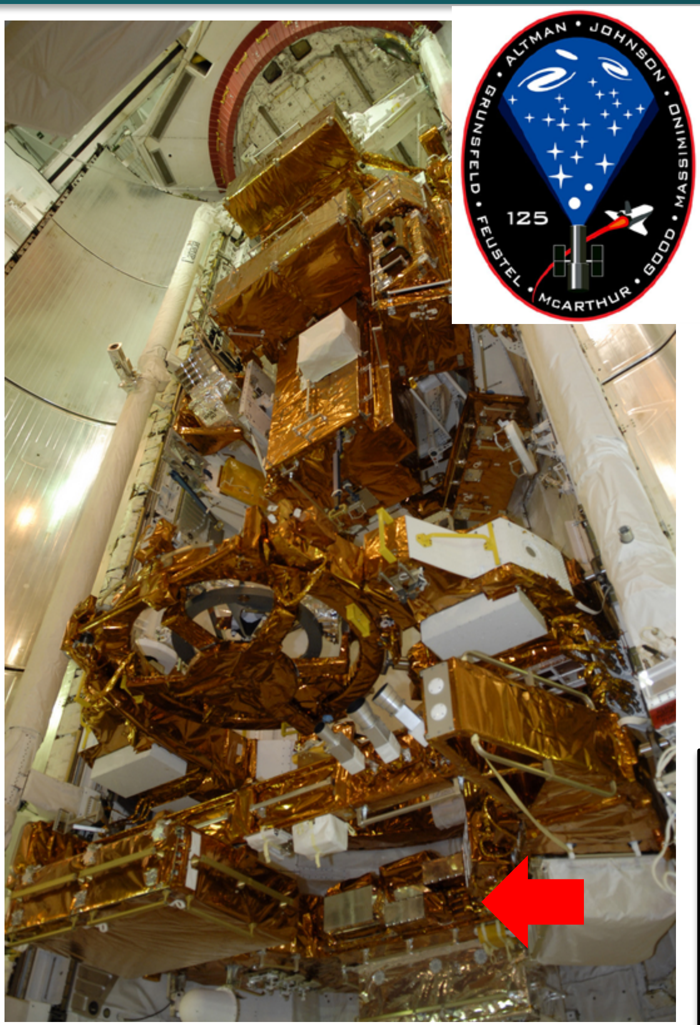
FPGA High-Level Design Example, RNS



Leveraged Mechanical, Electrical, FPGA Design, and Flight Software on each subsequent project

Reconfigurable System = Reduced $$ and Schedule

RNS Payload on HST-SM4, STS-125



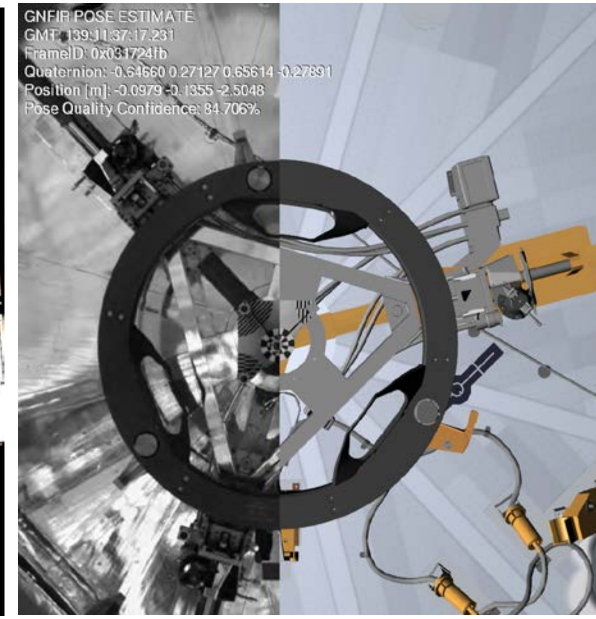
STS-125 Payload Bay

RNS System: 28 FPGAs

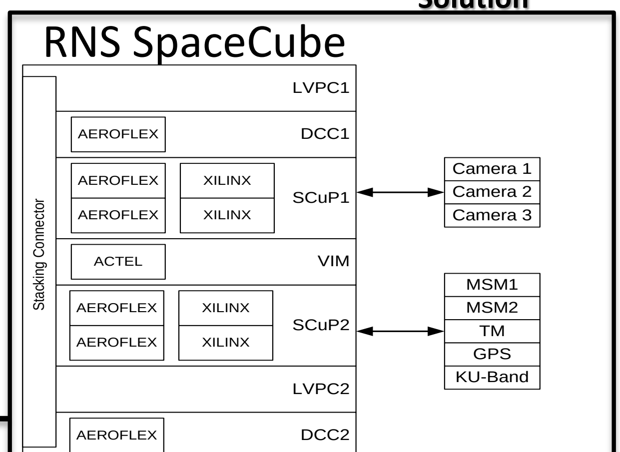
Long Range Camera on Rendezvous

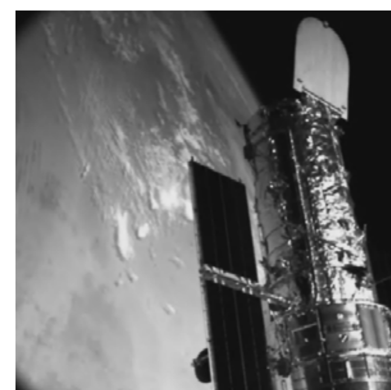
Flight Image | RNS Tracking Solution

Short Range Camera on Deploy



Flight Image | RNS Tracking Solution

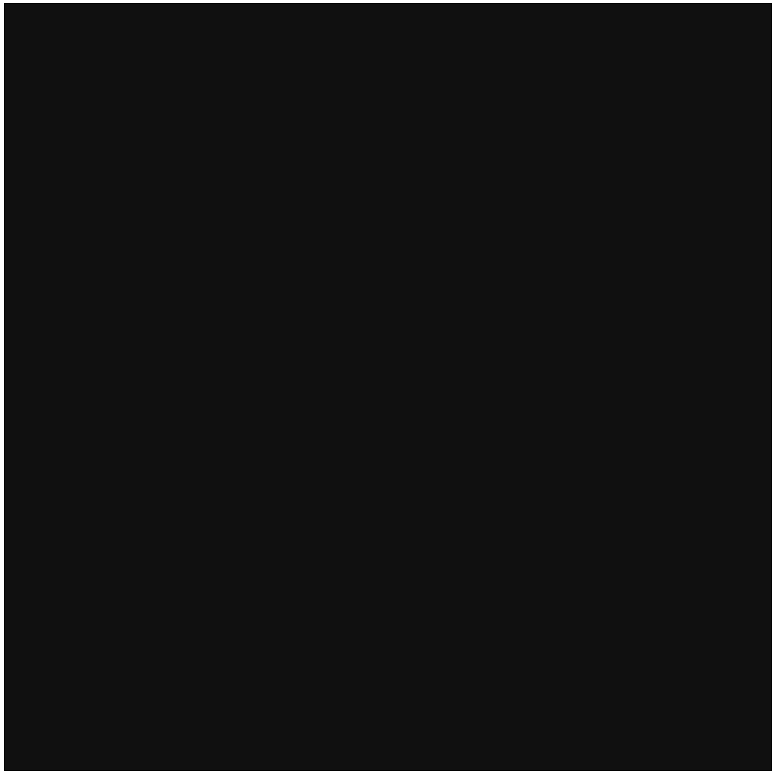




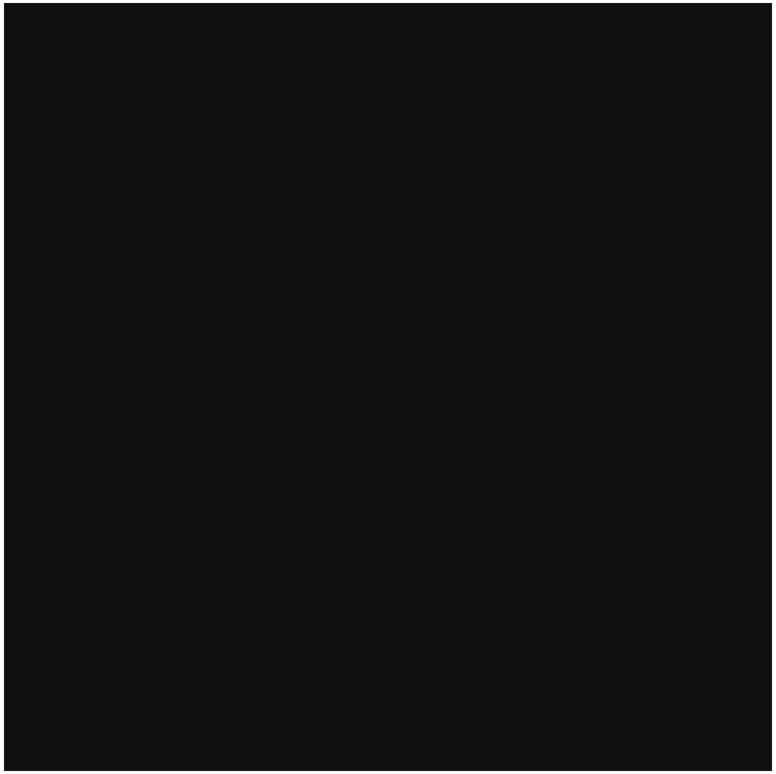
Compressed Image from HST Release

On-Board Image Processing

→ Successfully tracked Hubble position and orientation in real-time operations
→ FPGA algorithm acceleration was required to meet 3Hz loop requirement

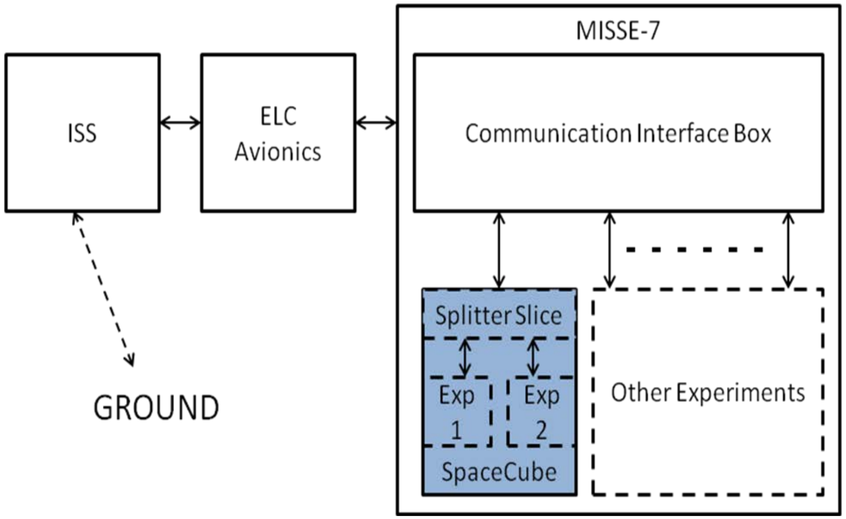


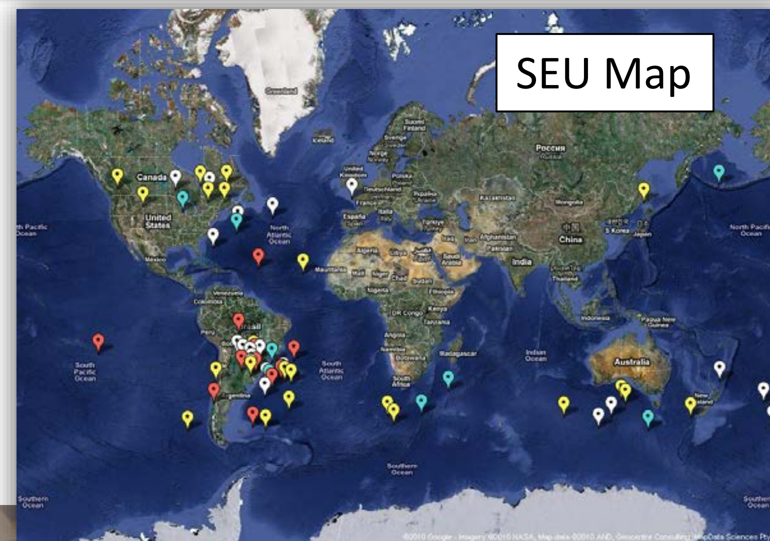
Rendezvous



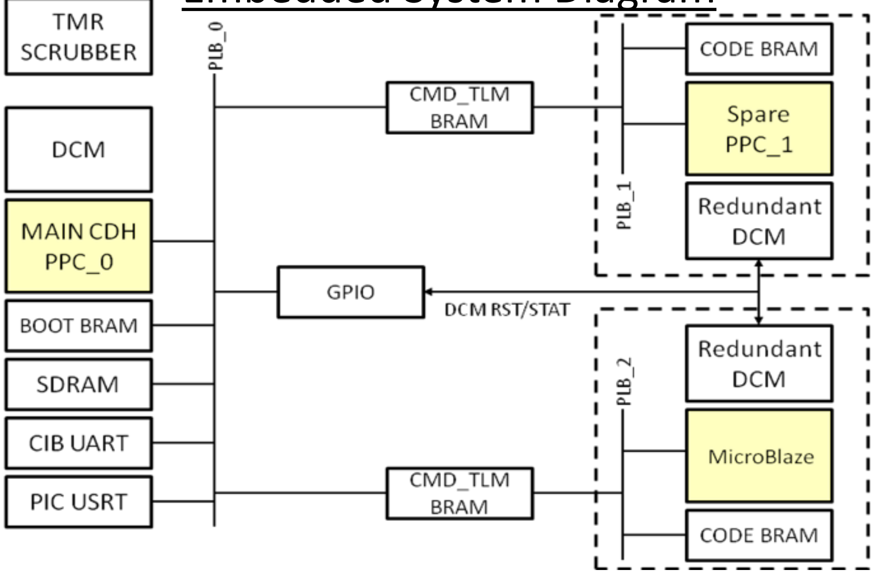
Deploy

MISSE7/8 SpaceCube





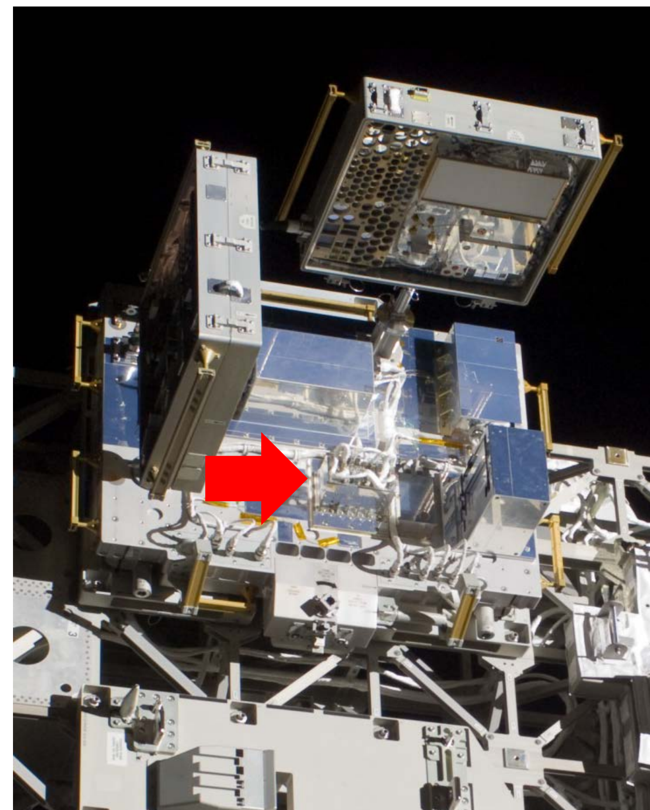
Embedded System Diagram



SpaceCube Upset Mitigation

GSFC SpaceCube v1.0 (Nov 2009):

- **"Radiation Hardened by Software" Experiment (RHBS)**
- **Autonomous Landing Application**
- **Collaboration with NRL and the DoD Space Test Program (STP)**

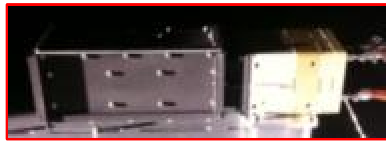


Data as of 3/1/2014

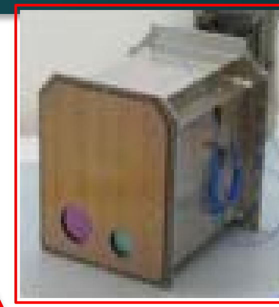
Days in orbit	**1500+**
Total SEUs detected & corrected	**200+**
Total SEU-induced resets	**6**
Total SEU-induced reset downtime	**30 min**
Total processor availability	**99.9979%**

Argon AR&D Test Payload

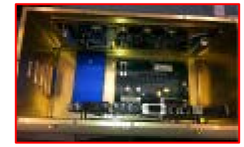
IR Camera



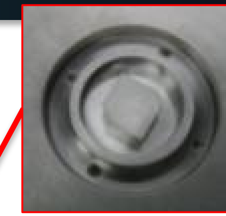
MDA RNS Cameras And Baffles



Ball VNS



Power Control Unit (PCU)



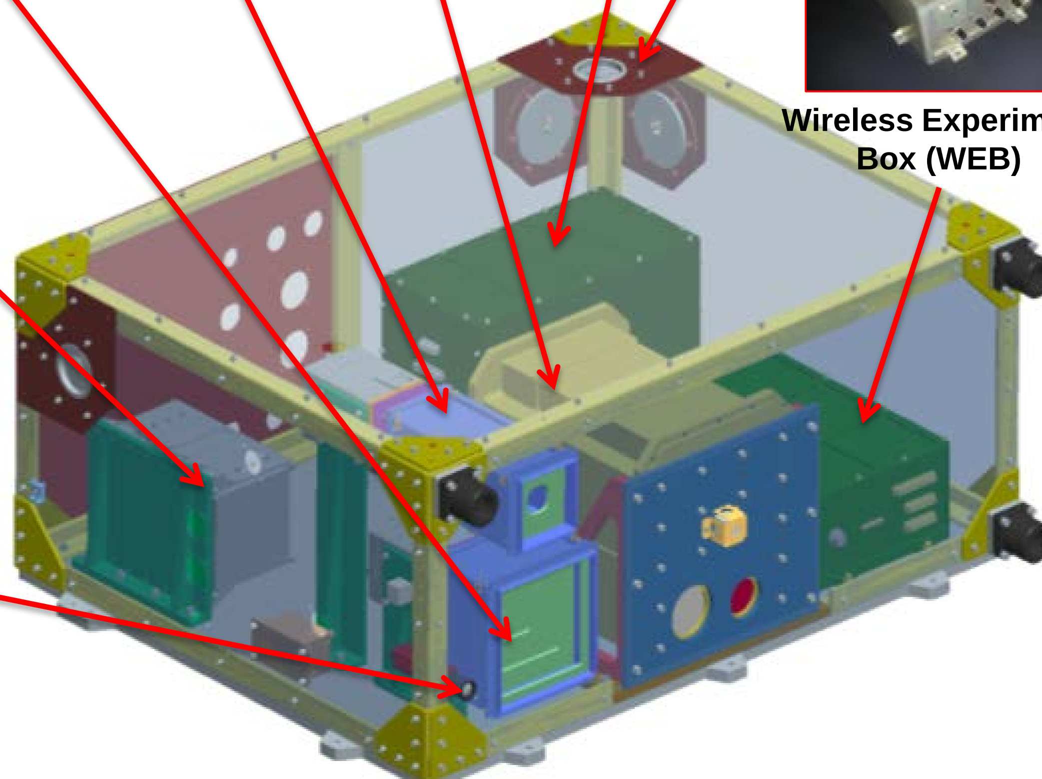
Wireless Patch Antennas (x4)

Wireless Experiment Box (WEB)

Neptec TriDAR

SpaceCube (EDU)

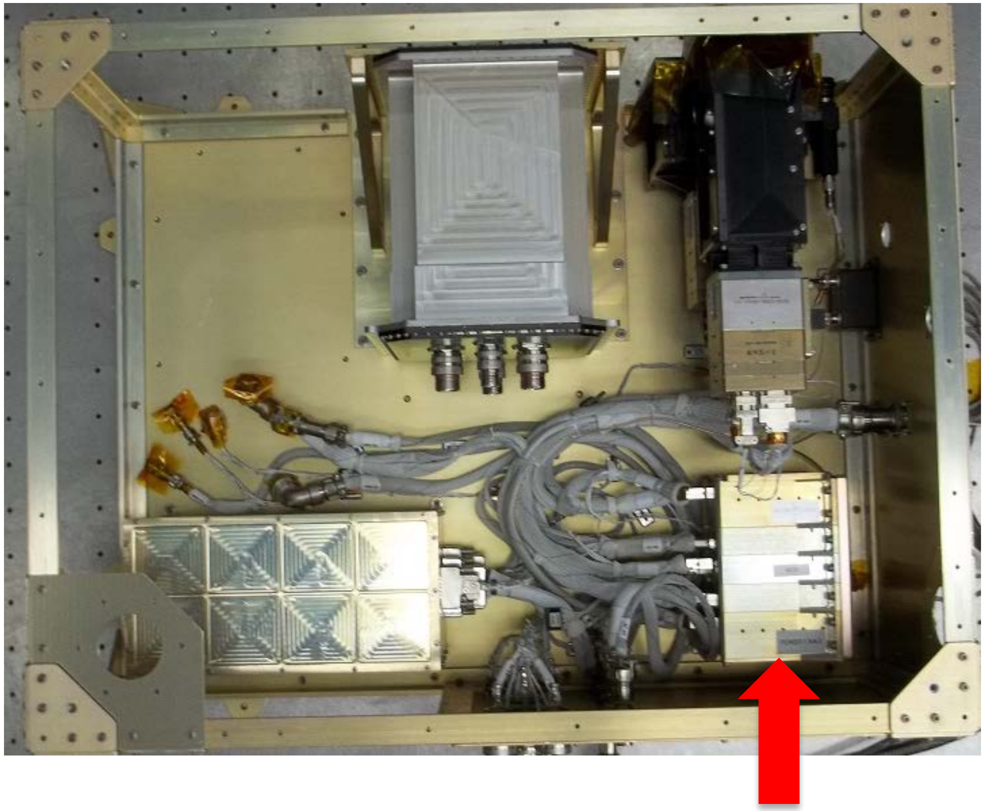
Ecliptic/Sony Situational Awareness Camera



Estimated Mass:
140 lb

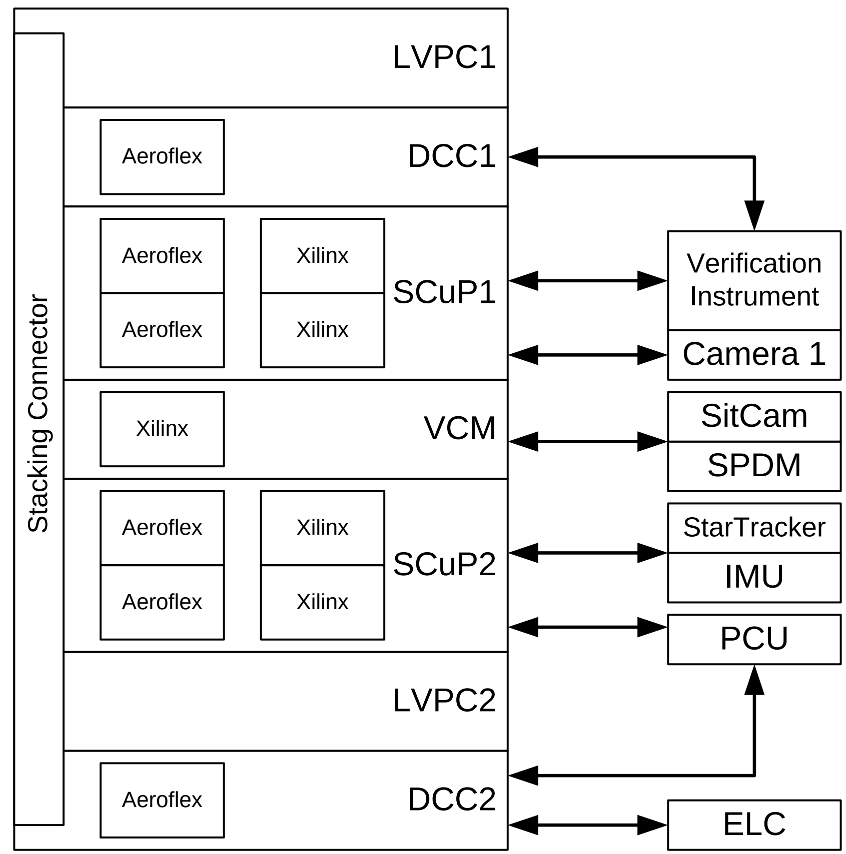
Rough Size:
25”x32”x14”

Argon Payload Assembly



SpaceCube

SpaceCube Interface Diagram



- → Embedded system consisted of 8 PowerPC405s
- → Reconfigurable system to support various instrument payloads

GSFC Satellite Servicing Lab

Testing with simulated 6-DOF motion of Argon and Target

- Rotopod and FANUC motion platforms simulate target-sensor dynamics
- Up to 13 m separation possible

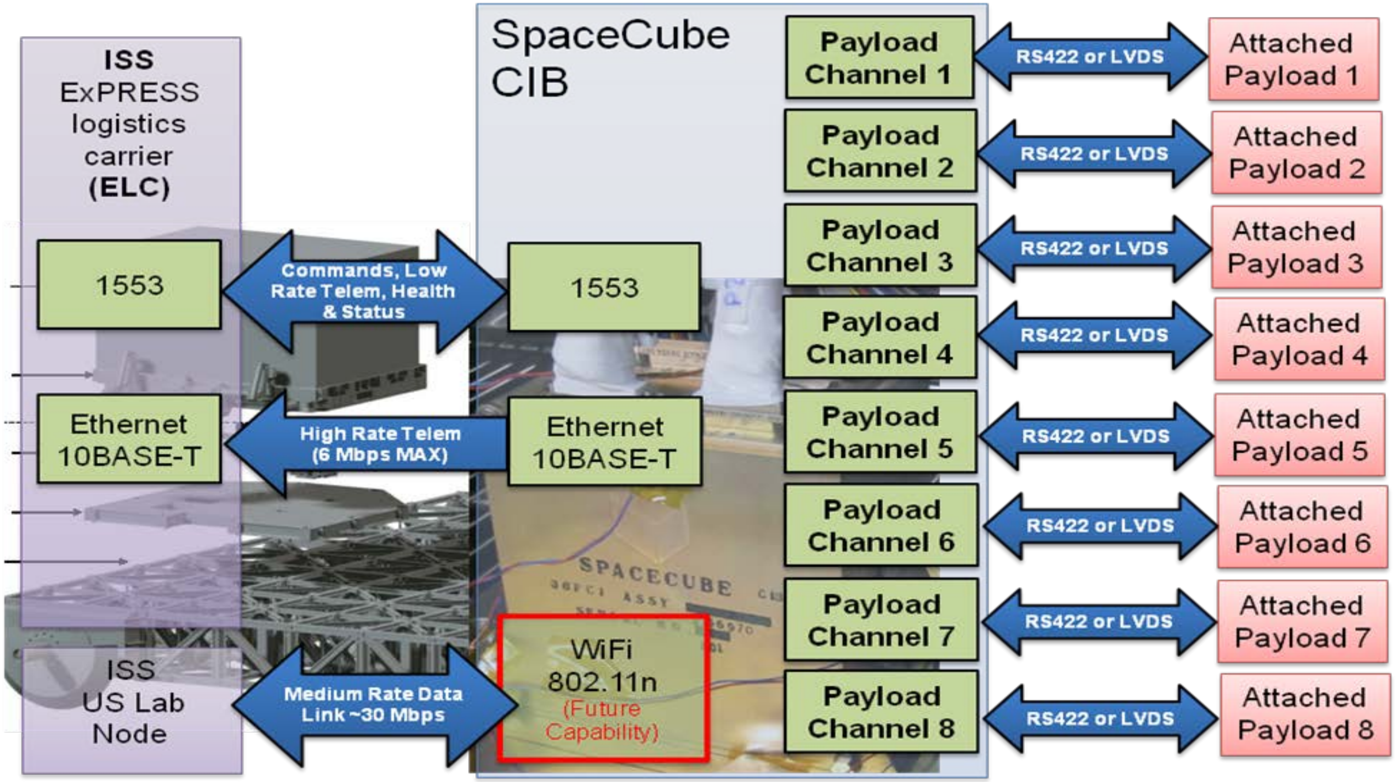
Testing conducted at GSFC in January-February 2012

- Motion includes closed-loop approach and non-cooperative “tumble”
- Open loop testing to characterize sensor/algorithm performance
- Closed-loop tests - evaluate end-to-end system (sensors, algorithms, control law) in real time

SpaceCube CIB, STP-H4

- Delivery to Space Test Program
- Interfaces with ELC and 8 attached payloads

→ **Reflight of RNS Hardware**



Days in orbit	**200+**
Total SEUs detected & corrected	**20+ (as of 3/1/2014)**
Total SEU-induced resets	**1**

ISS SpaceCube Experiment 2.0

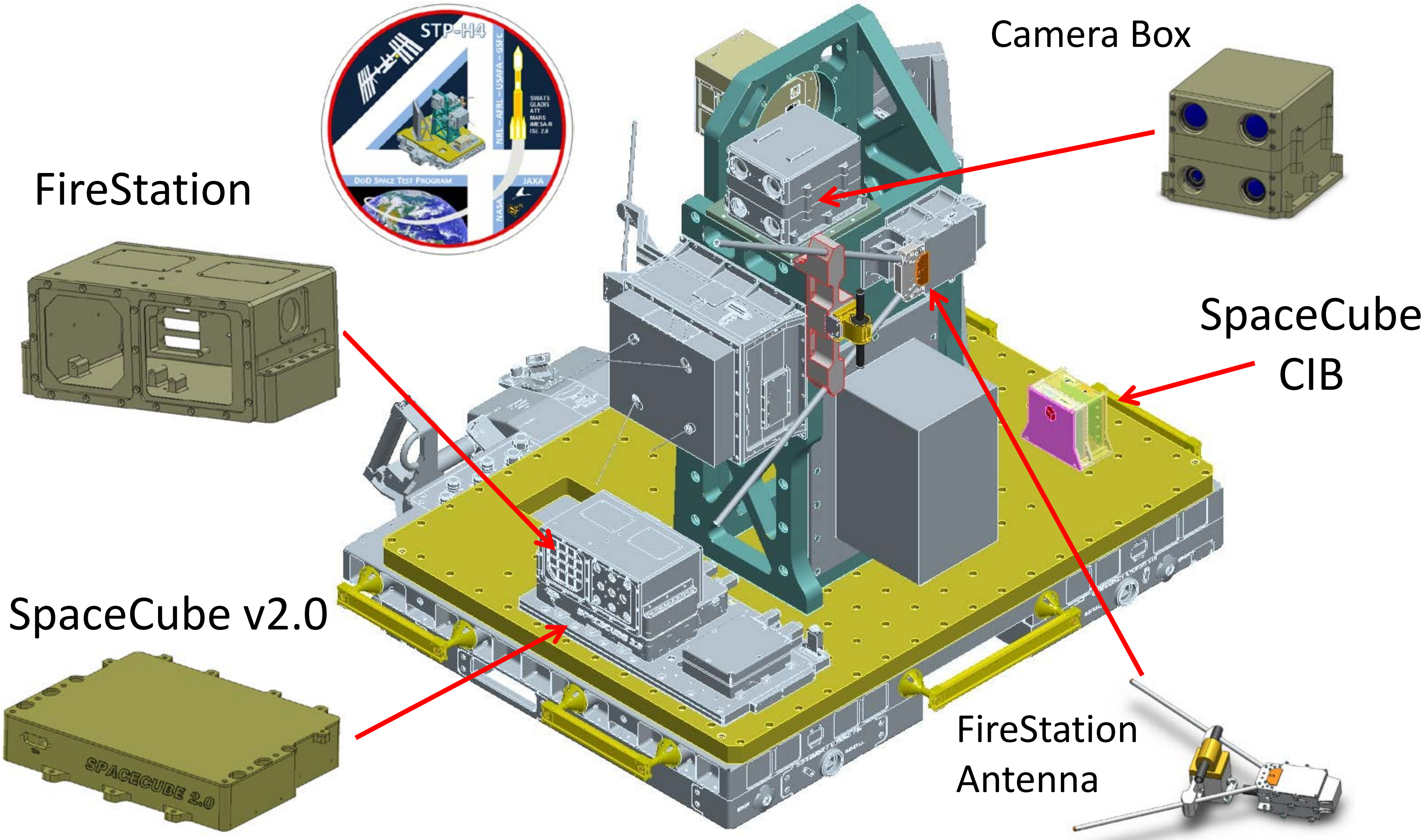
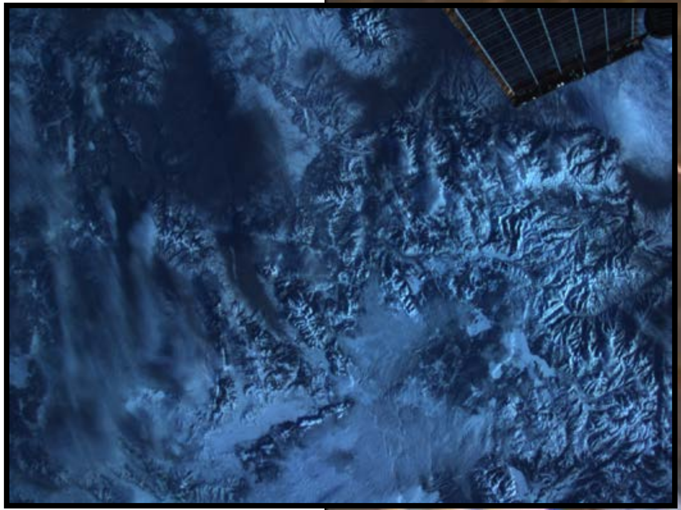
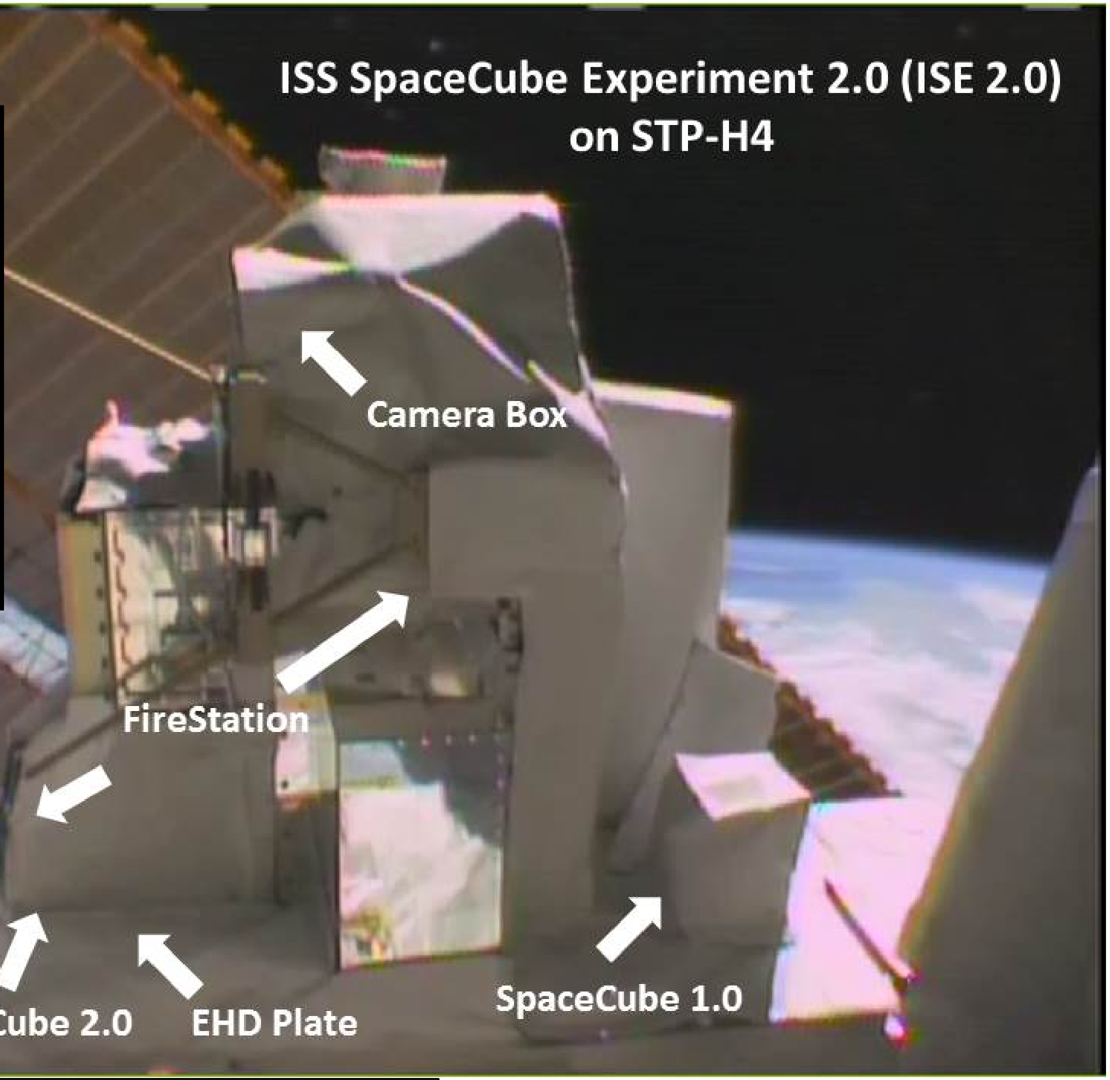


Image Credit: DoD Space Test Program

STP-H4 Operational on ISS

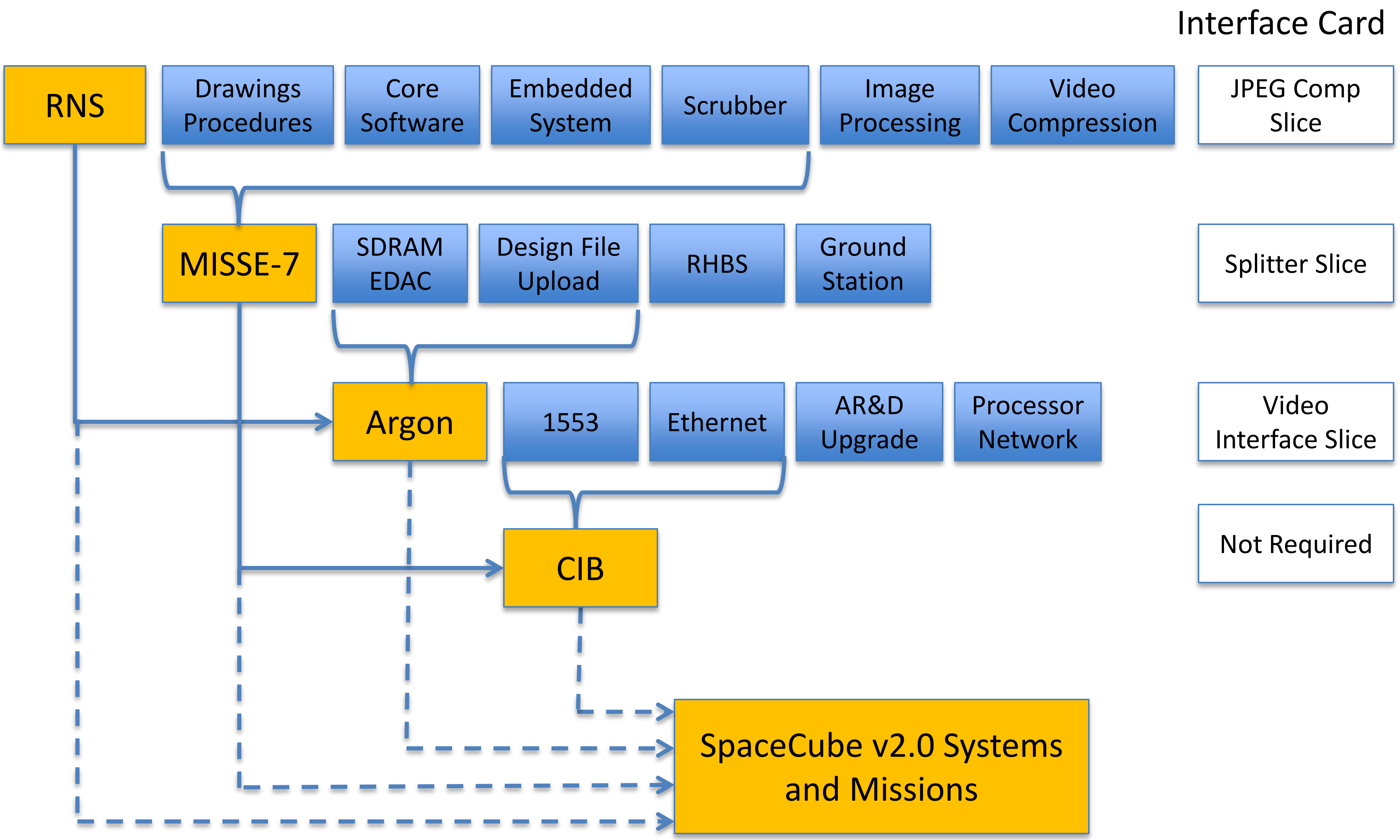


Somewhere near Big Sky

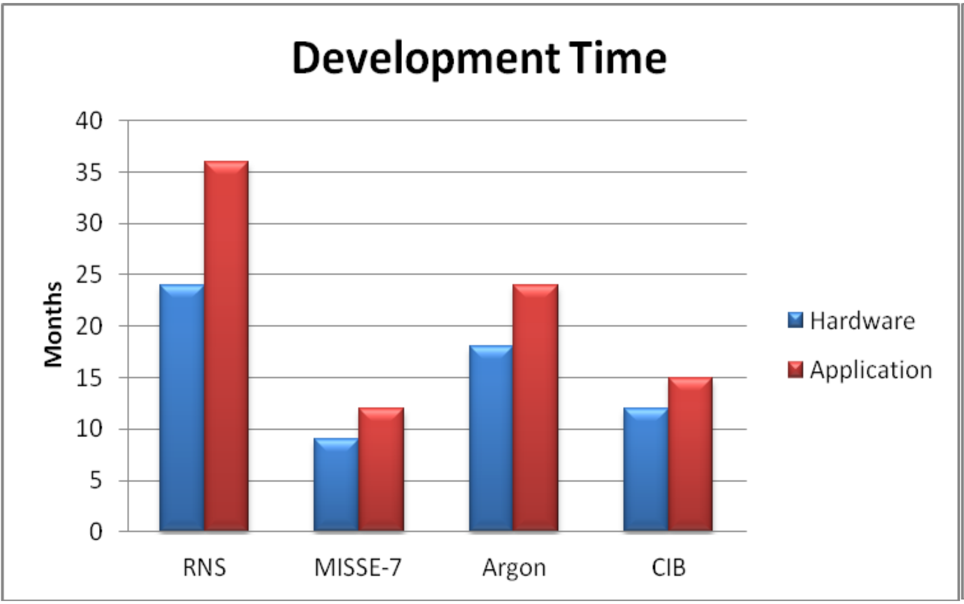


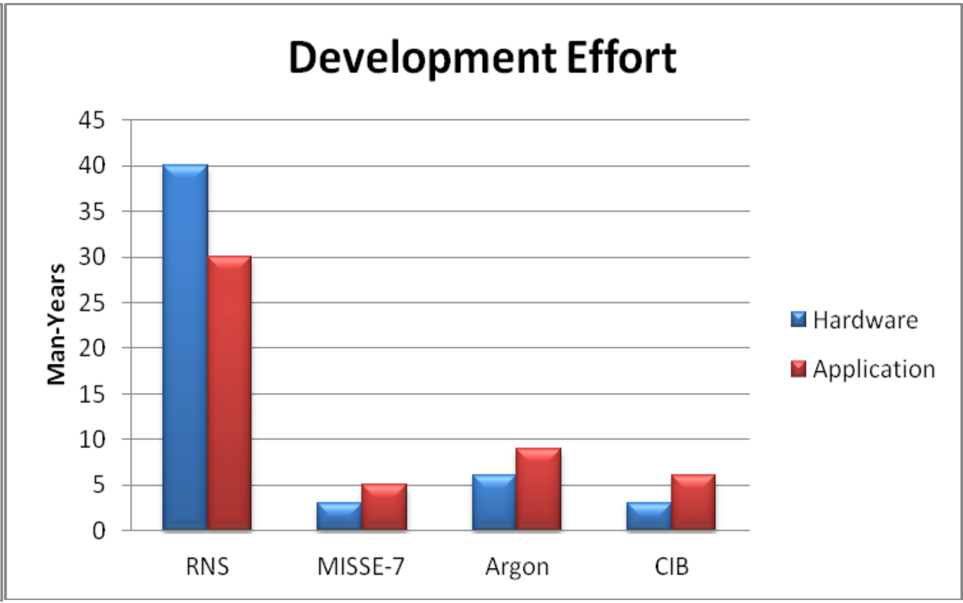
Next Up: STP-H5 and Robotic Refueling Mission 3 in 2015

System Reuse and Reconfiguration



Conclusions





→Designing a new system has significant non-recurring engineering cost
→Solid embedded system infrastructure and reconfigurable file structure is critical
→A reconfigurable and adaptable system enables low-cost, quick-turn missions
→A scalable mechanical/electrical system can easily adapt to new interface requirements
→Reconfigurable system enables accelerated requirements creep