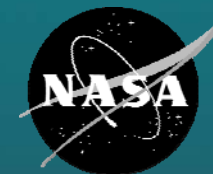


National Aeronautics and Space Administration



SpaceCube v2.0 Space Flight Hybrid Reconfigurable Data Processing System

2014 IEEE Aerospace Conference

Track 7.01:

High Performance Space Processing and High-Speed Performance Satellite Architectures and Standards

Dave Petrick

Embedded Systems Group Leader

SCIENCE DATA PROCESSING BRANCH
Code 587 • NASA GSFC

www.nasa.gov

SpaceCube



SpaceCube, Target Applications

- Small, light-weight, reconfigurable multi-processor platform for space flight applications demanding extreme processing capabilities
 - Reconfigurable components: FPGA, Software, Mechanical
 - Promote reuse between applications
- Hybrid Flight Computing: hardware acceleration of algorithms to enable onboard data processing and increased mission capabilities
- Example Applications: Instrument Data Interfacing and On-Board Processing, Autonomous Operations, Situational Awareness, Scalable Computing Architectures

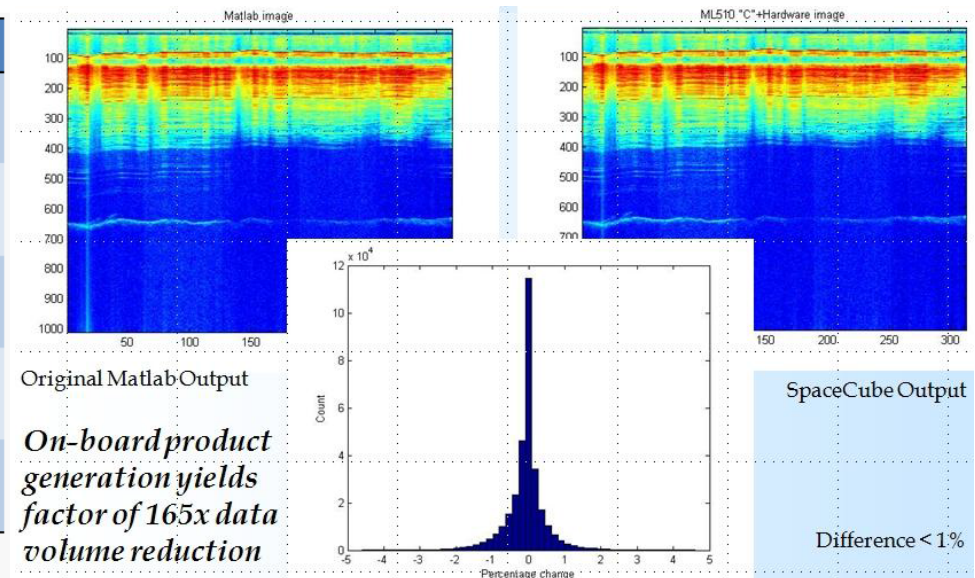
Hardware Algorithm Acceleration

Application	Xilinx Device	Acceleration vs CPU
SAR	Virtex-4	79x vs PowerPC 405
Altimeter	FX60	(250MHz, 300 MIPS)
RNS GNfir	Virtex-4	25x vs PowerPC 405
FPU, Edge	FX60	(250MHz, 300 MIPS)
HHT	Virtex-1	3x vs Xeon Dual-Core
EMD, Spline	2000	(2.4GHz, 3000 MIPS)
Hyperspectral Data	Virtex-1	2x vs Xeon Dual-Core
Compression	1000	(2.4GHz, 3000 MIPS)
GOES-8 GndSys	Virtex-1	6x vs Xeon Dual-Core
Sun correction	300E	(2.4GHz, 3000 MIPS)

Notes:

- 1) All functions involve processing large data sets (1MB+)
- 2) All timing includes moving data to/from FPGA
- 3) SpaceCube 2.0 is 4x to 20x more capable than these earlier systems

On-Board Data Reduction



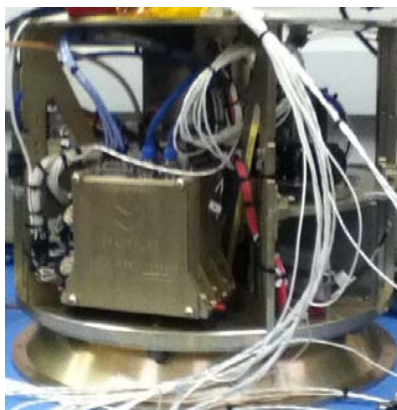
SpaceCube Family Overview

v1.0



2009 STS-125
 2009 MISSE-7
 2013 STP-H4
 2015 STP-H5

v1.5



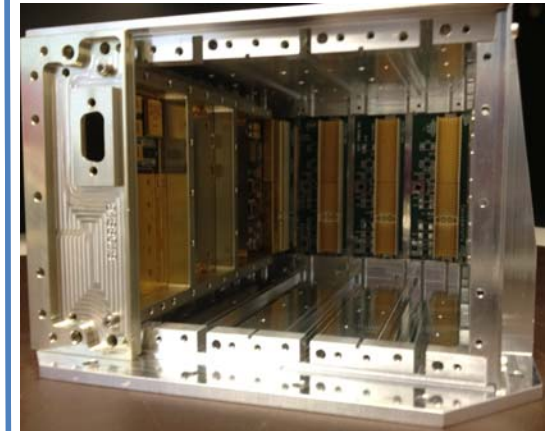
2012 SMART

v2.0-EM



2013 STP-H4
 2015 STP-H5

v2.0-FLT

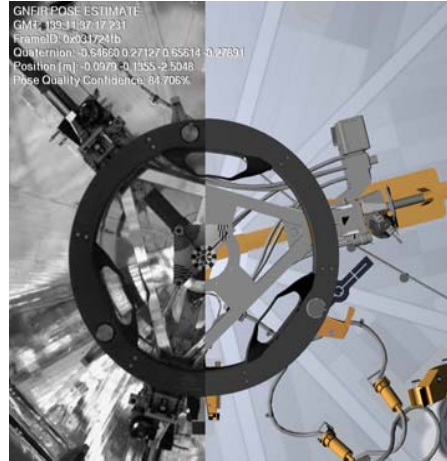


2015 GPS Demo
 - Robotic Servicing
 - Numerous proposals
 for Earth/Space/Helio

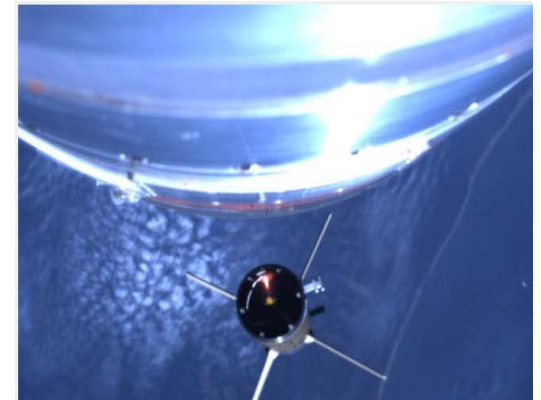
Example SpaceCube Processing



Real-Time Image Tracking of Hubble



Fire Classification



Gigabit Instrument Interfacing

Xilinx ISS Radiation Data



Spectrometer Data Reduction

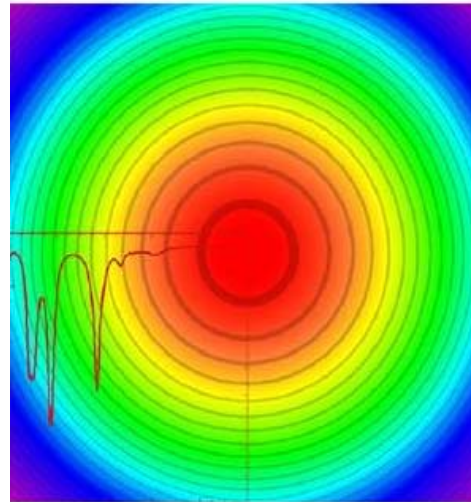
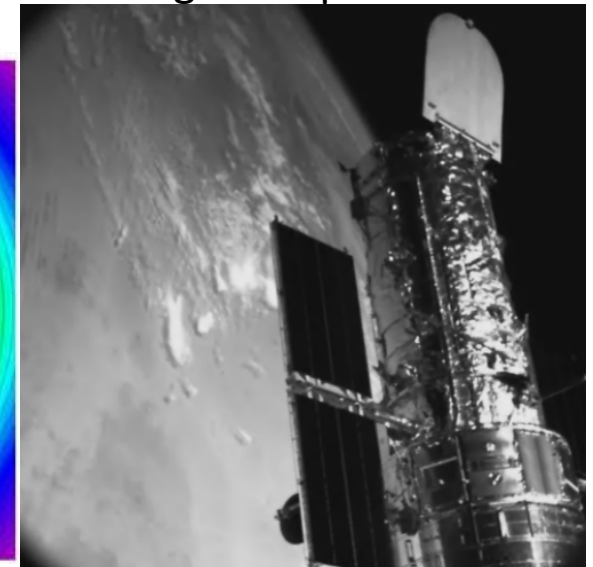


Image Compression

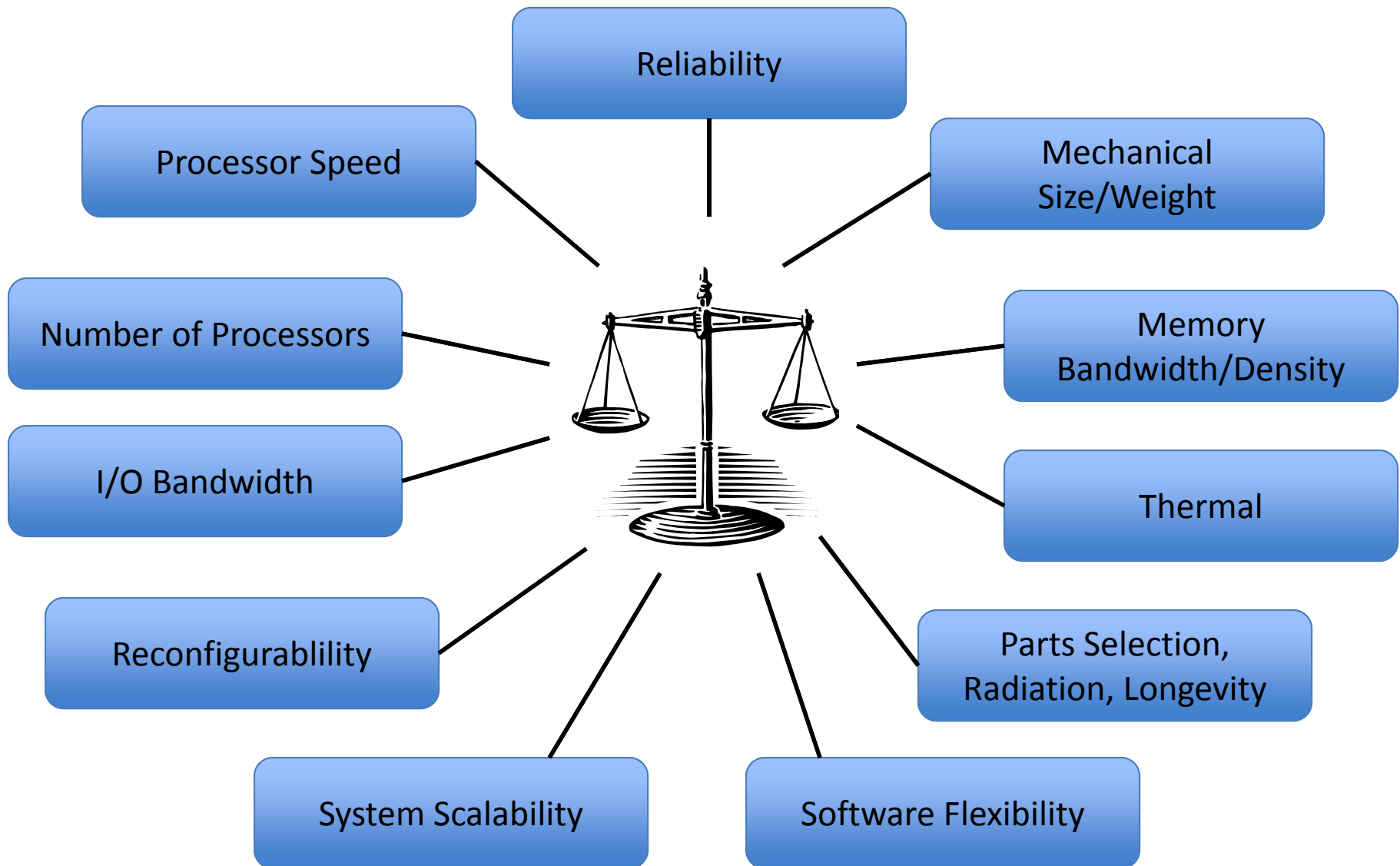


High Performance Space Processing System

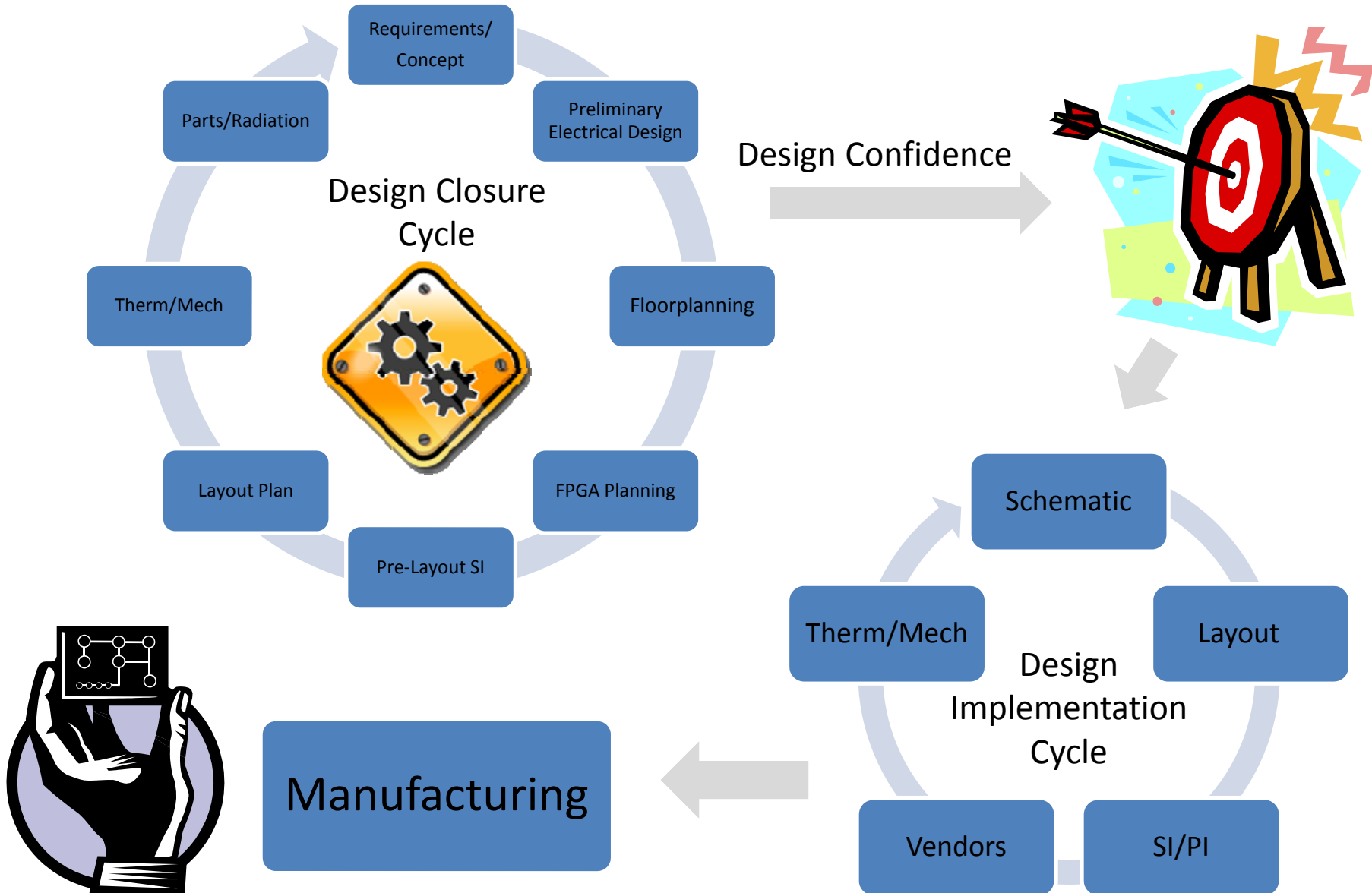
- What defines a “High Performance Space Processing System”?
 - Memory bandwidth and density, processing speed, reconfigurable, number of processors, I/O bandwidth, scalable, power, size and weight, temperature range, reliability, radiation, software flexibility
 - Mission Context: differing driving requirements
- Problem: All of these system variables push against each other
 - Not taking the time to fully understand the dynamics between these variables will result in an unoptimized, inefficient design
- Our Solution: SpaceCube v2.0
 - Design Methodology
 - Pushes all edges of technology for space flight
 - Maintains excellent reliability standards



Balanced Design Closure of System Variables

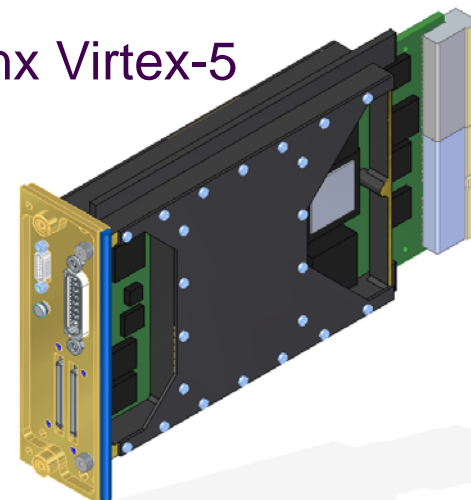


Design Flow for Constrained System

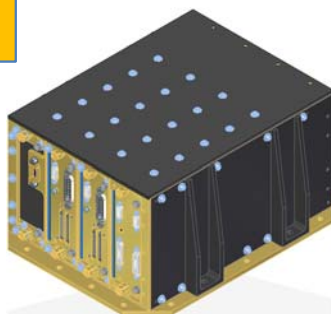
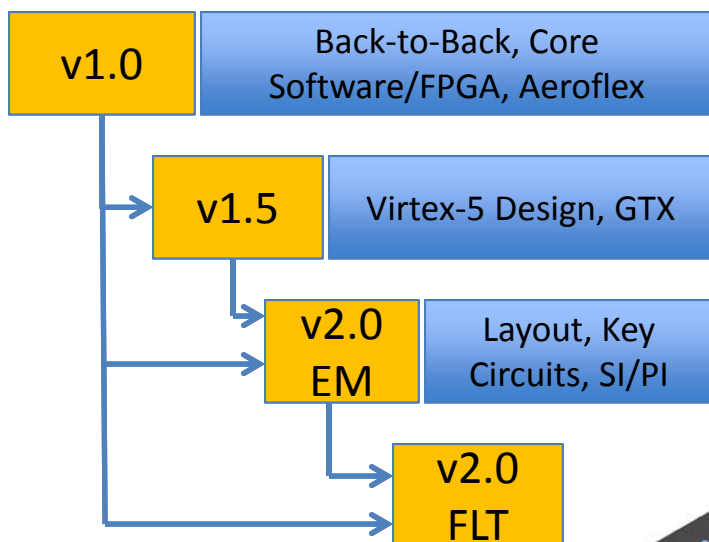


SpaceCube v2.0 System

- Reconfigurable multi-processing platform based on Xilinx Virtex-5 FPGAs
- Extended 3U Compact PCI mechanical standard



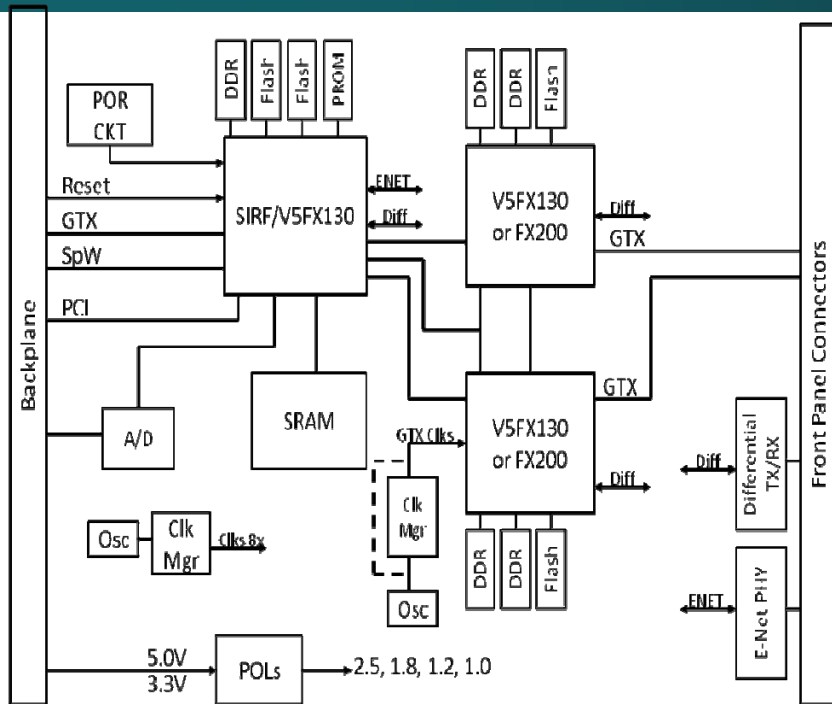
Design Heritage



Processor Comparison

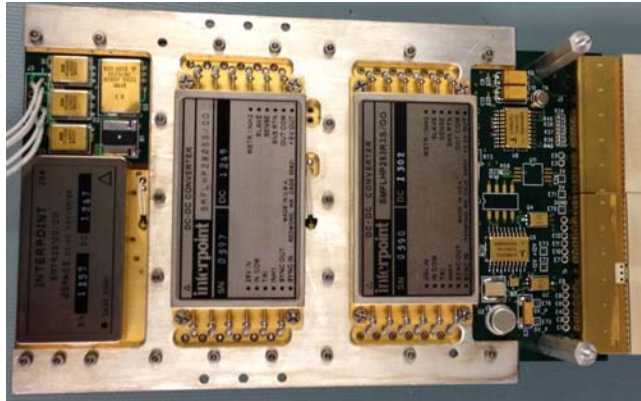
Processor	MIPS	Power	MIPS/W
MIL-STD-1750A	3	15W	0.2
RAD6000	35	15W	2.33
ColdFire	60	7W	8
RAD750	250	14W	18
LEON 3FT	89	5.5W	16
LEON3FT Dual-Core	200	10W	20
BRE440 (PowerPC)	266	5W	53
Maxwell SCS750	1200	25W	48
SpaceCube 1.0	3000	7.5W	400
SpaceCube 2.0			
PowerPC (4x)	5000	9W	550
MicroBlaze (4x)	600	8W	75
SpaceCube Mini	2500	5W	400

v2.0 Processor Engineering Model



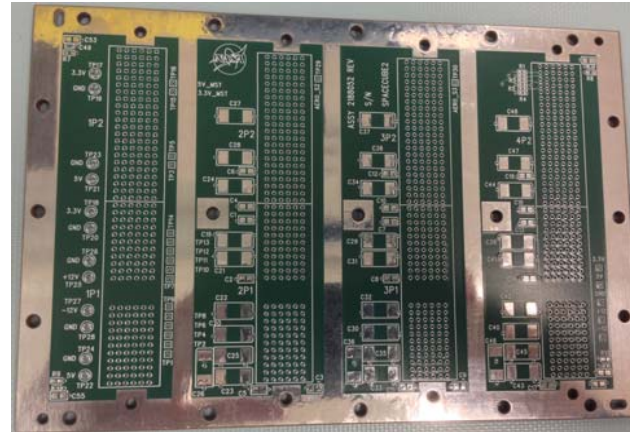
- 6U Board Design board layout to simulate a 3U layout for major components
- Test sample circuits, layout techniques, and interfacing architectures
- Roll lessons learned into flight system
 - Back-to-Back layout strategy for all like parts
 - Signal integrity solutions
 - Oscillator and power architecture
 - Connector selection
 - Unique layout strategy for accomplishing IPC 6012B Class 3/A PWB

SpaceCube v2.0 Flight System



Power Card

- 22-38V Input, 7A limit
- 5V/80W, 3.3V/53W, +/-12V/24W

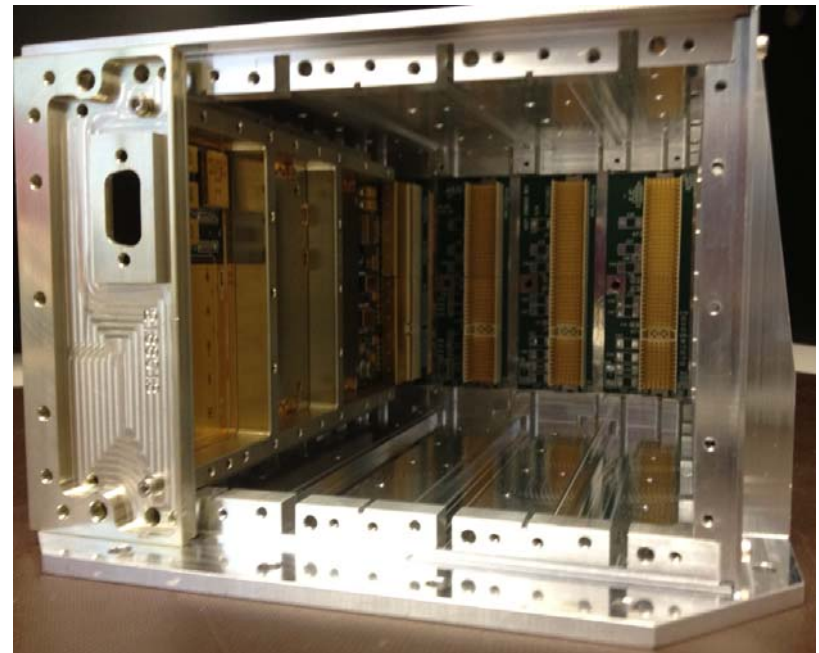


Backplane Card

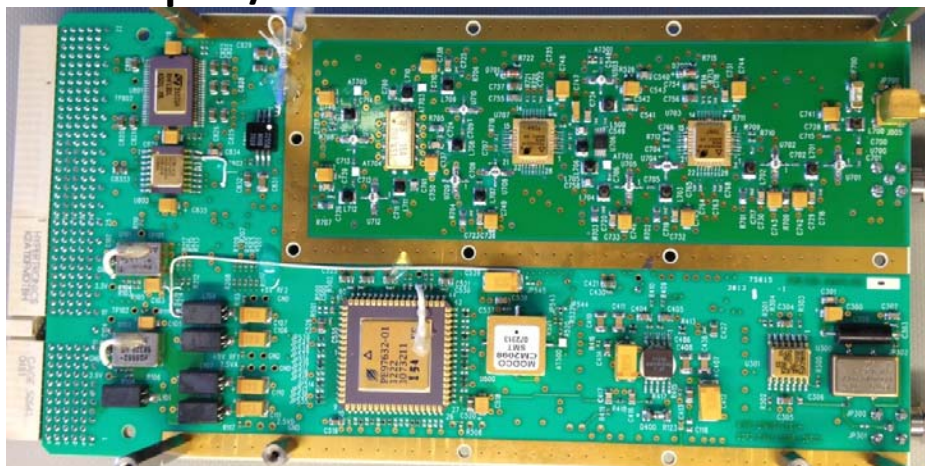
- 4 slots
- Point-to-Point
- Gigabit
- 2 processors, 1 I/O
- 3 processors



Chassis: 12.7 x 23 x 27 cm³



Example I/O Card: GPS RF



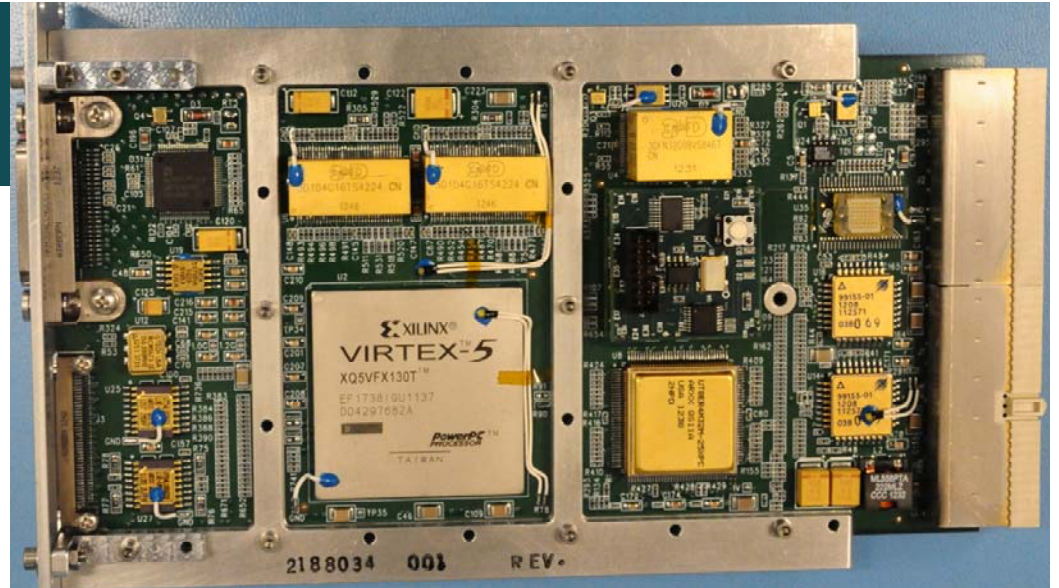
Processor Card

Power Draw: 6-12W

Weight: 0.98-lbs

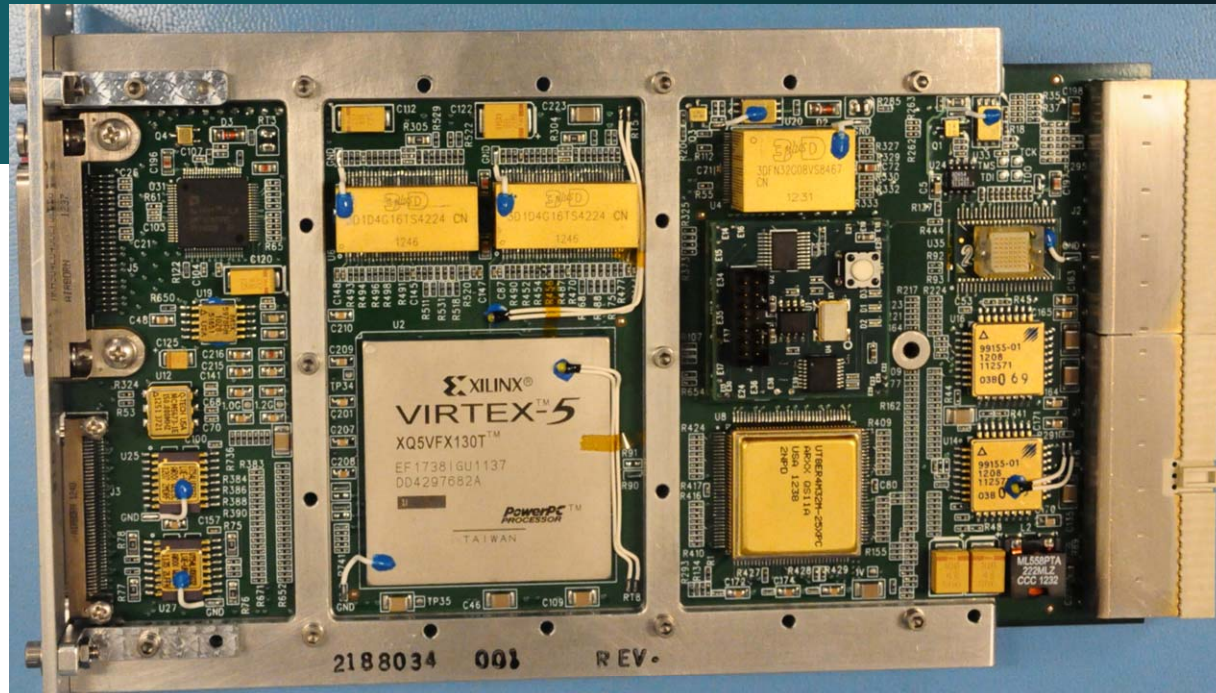
22 Layers, Via-in-Pad

IPC 6012B Class 3/A

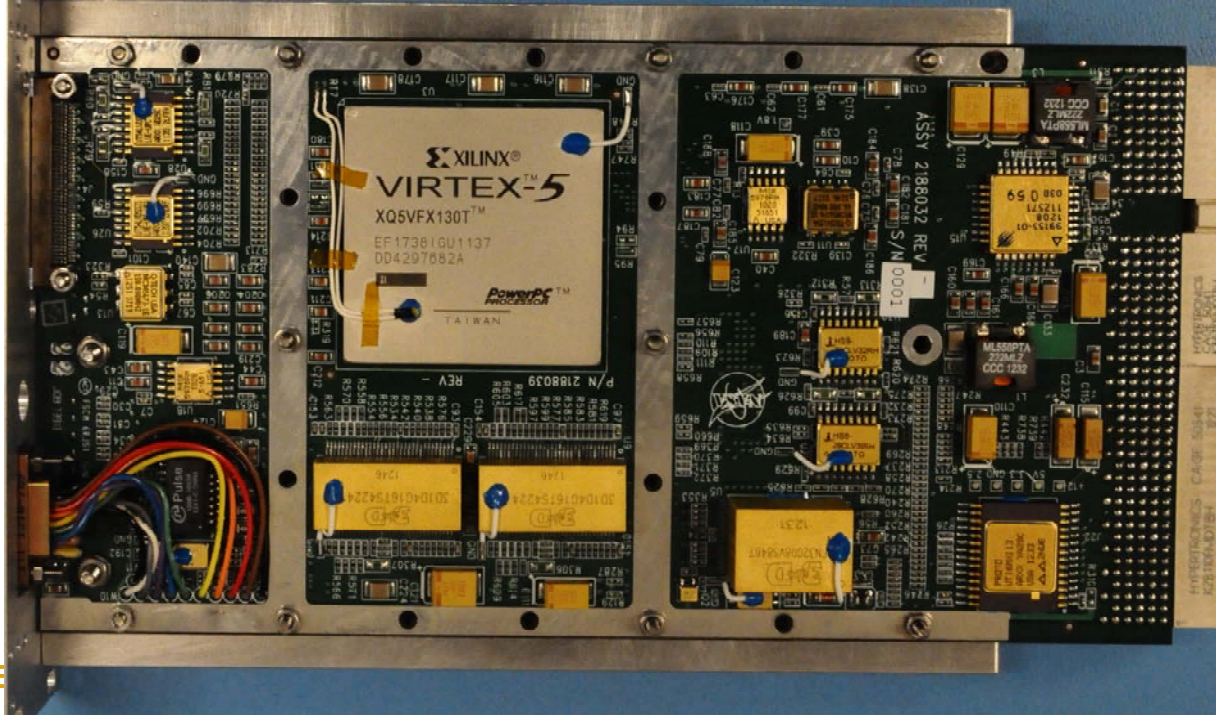


- 2x Xilinx Virtex-5 (QV) FX130T FPGAs
- 1x Aeroflex CCGA FPGA
 - Xilinx Configuration, Watchdog, Timers
 - Auxiliary Command/Telemetry port
- 1x 64Mb PROM, contains initial Xilinx bitfile (will also support 128Mb PROM)
- 1x 16MB SRAM, rad-hard with auto EDAC/scrub feature
- 4x 512MB DDR SDRAM
- 2x 4GB NAND Flash
- 16-channel Analog/Digital circuit for system health
- Optional 10/100 Ethernet interface
- Gigabit interfaces: 4x external, 2x on backplane
- 12x Full-Duplex dedicated differential channels
- 88 GPIO/LVDS channels directly to Xilinx FPGAs
- Mechanical support for heat sink options and stiffener for Xilinx devices

TOP



BOTTOM

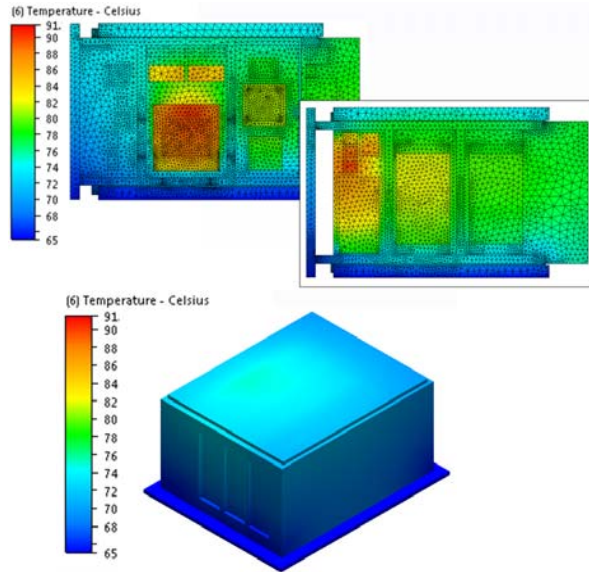


SCIE

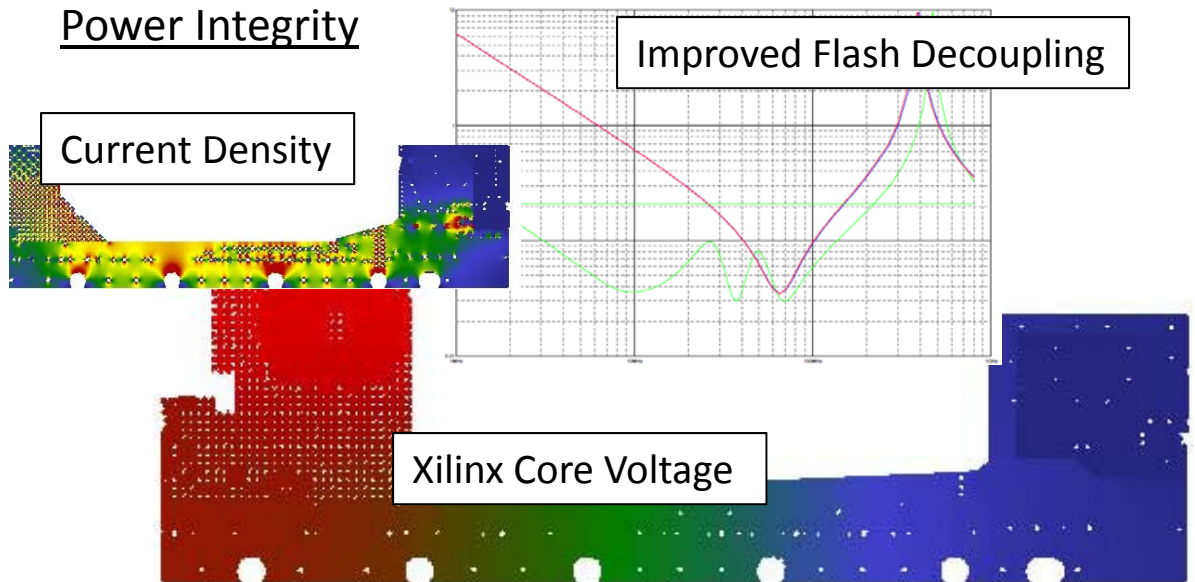
SFC

Design Analysis

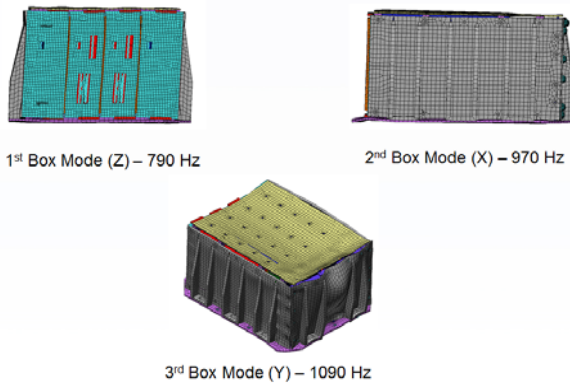
Thermal: -40°C to 65°C



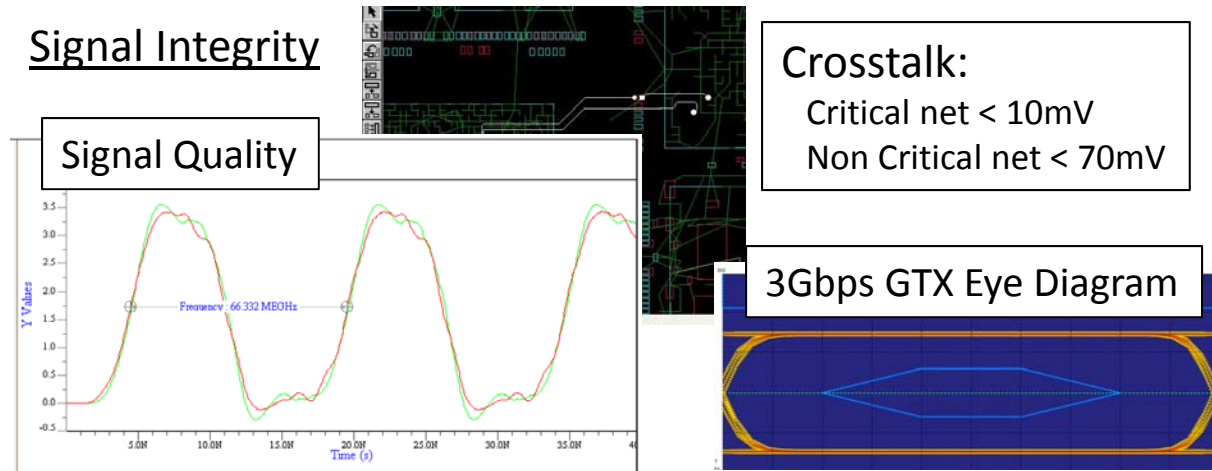
Power Integrity



Structural



Signal Integrity



ISS SpaceCube Experiment 2.0

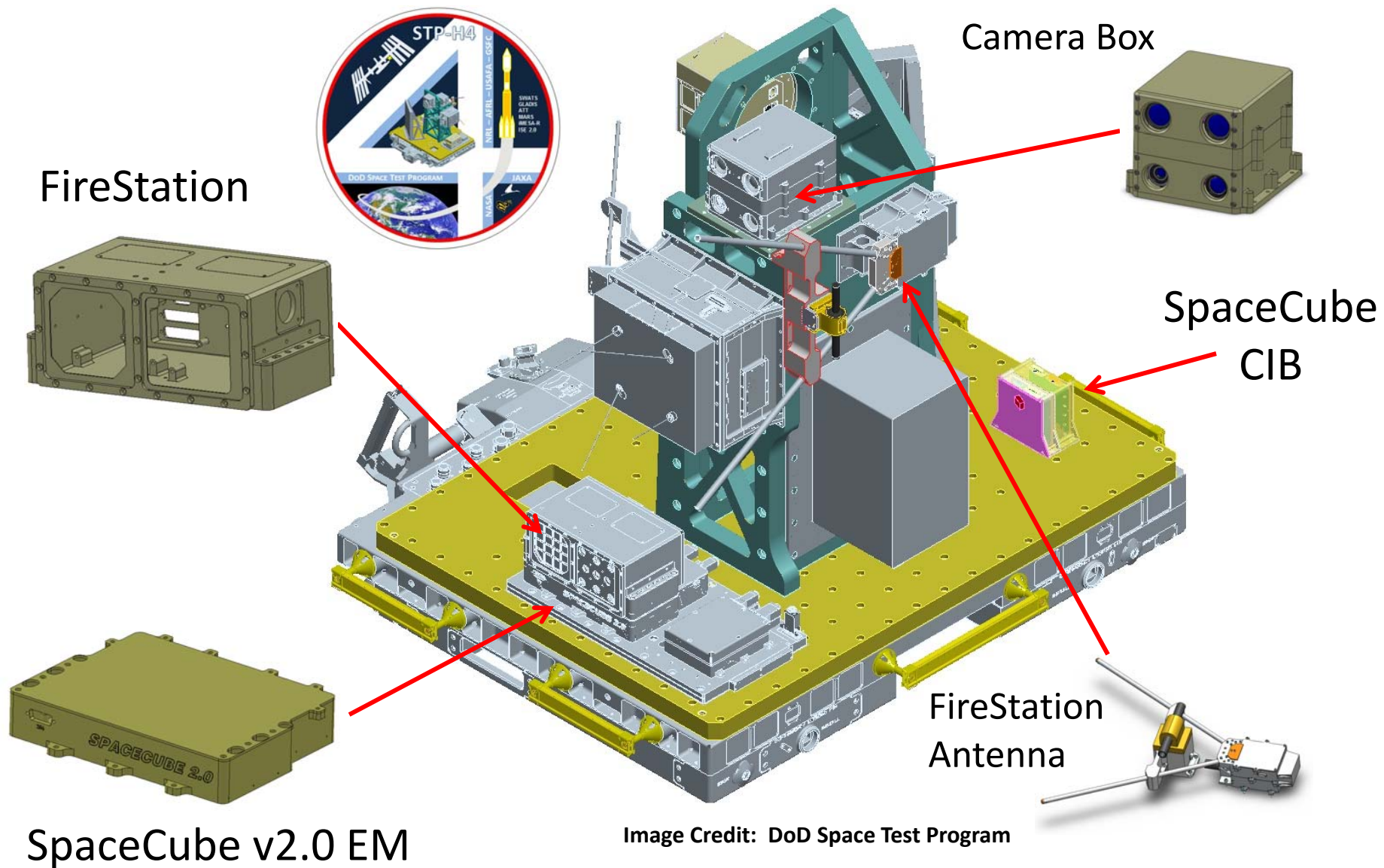
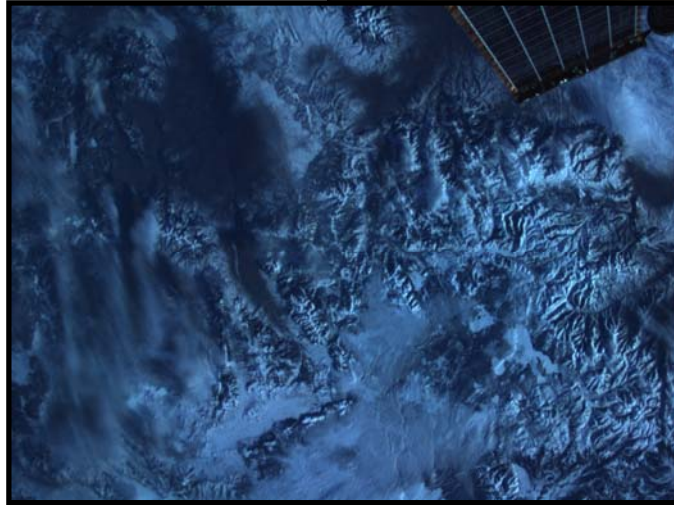
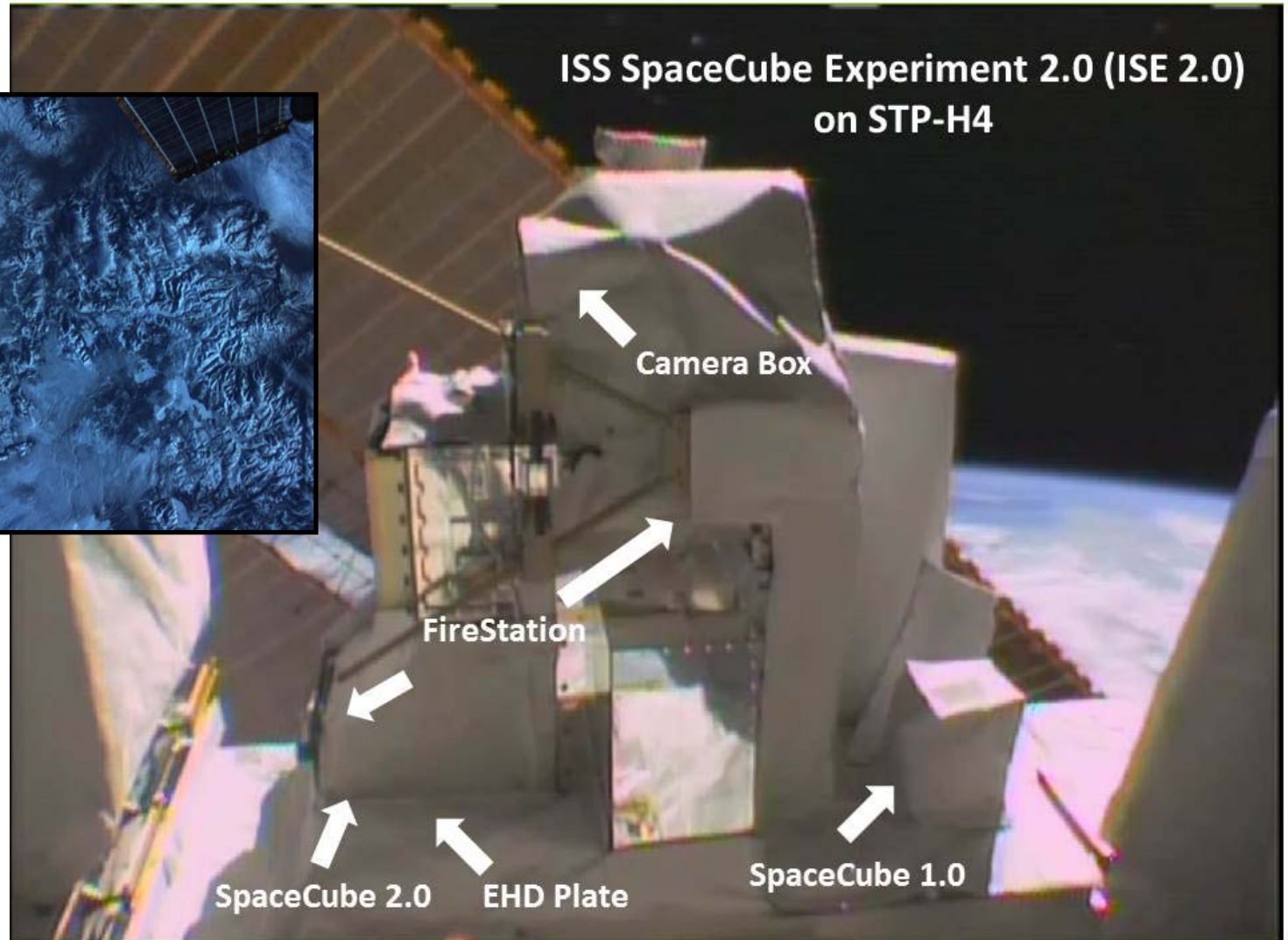


Image Credit: DoD Space Test Program

STP-H4 Operational on ISS



Somewhere near
Big Sky, MT



Next Up: STP-H5 and Sounding Rocket Launch in 2015

ISE2.0 Results

Operations

- GSFC Command Center
- August 2013 - Present

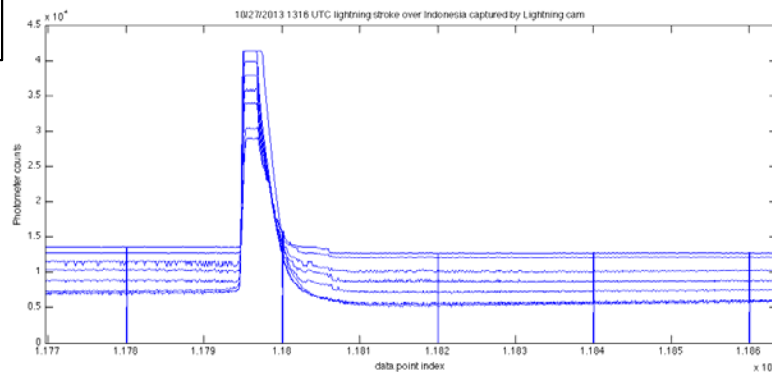
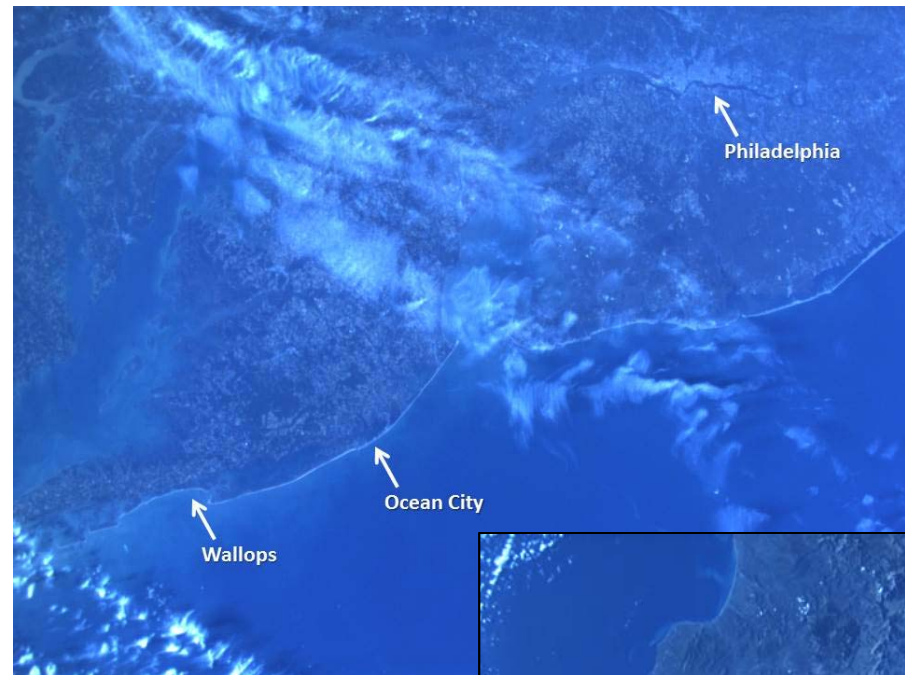
Radiation

FPGA	SEUs
1	23
2	21
3	30

~1 SEU/FPGA/Week
FPGA Resets: 3

FireStation Instrument
Data Processing

HD Images Received: 200,000+



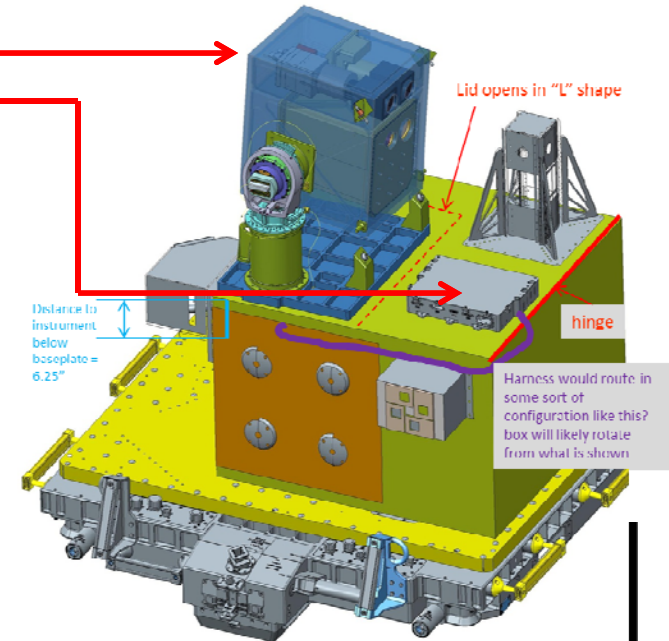
Satellite Servicing

STP-H5 Autonomous Rendezvous and Docking Payload

- SpaceCube v2.0 EM
- Leverages SpaceCube v1.0 RNS/Argon demonstrations

Objective: Robotic Satellite Servicing Mission

- SpaceCube v2.0 Flight System
- 2 Processors/SpaceCube
- 3 SpaceCubes controlling AR&D and robotic tasks



GSFC Satellite Servicing Laboratory

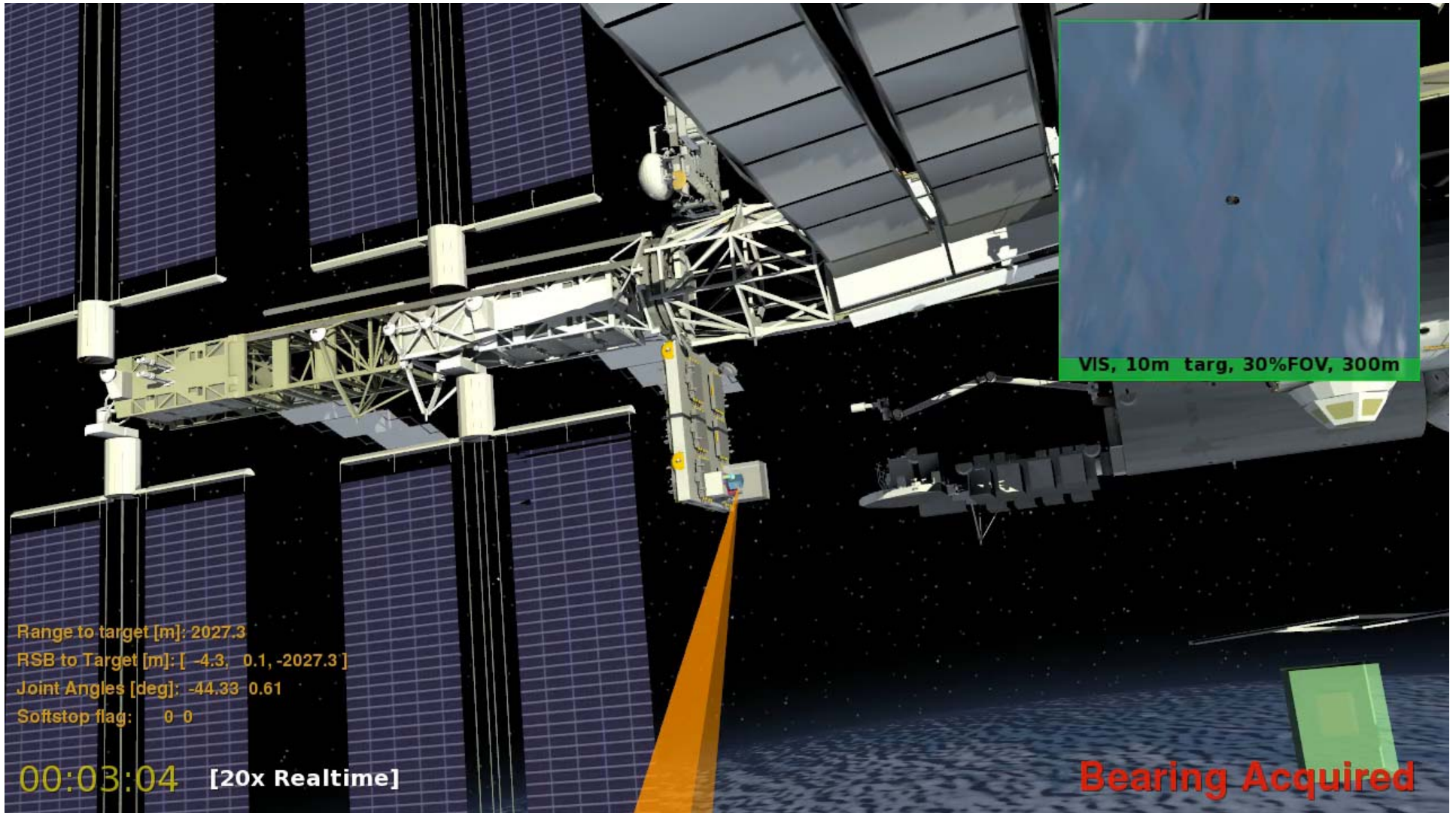


Argon with SpaceCube v1.0 Control



GOES-12 Model

Raven ConOps



Conclusions

- An advanced HPC for space requires well balanced system variables
- Imperative to iterate on design plan before starting schematics
 - No use starting something that will not close on requirements
 - System Designer: Know what you want to build, and how to build it
 - Pull all disciplines into design cycle at the beginning
- SpaceCube design methodology successful in converging on a cutting-edge HPC design given constrained size requirements
 - SWaP = \$\$ → Make it smaller!!!
 - Back-to-Back parts placement
 - Extensive analysis
 - Built to high reliability standards
- SpaceCube v2.0 Flight System
 - Design heritage leveraged from 3 prior systems
 - Operations heritage leveraged from 5 flights
 - By 2015, 9 SpaceCube systems flown → 22 Xilinx FPGAs in space
 - Competitive HPC for space
 - Multiple mission applications, reconfigurable