Application of SpaceCube in a Space Flight System

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Code 587

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Note: This is the HANDOUT version of this presentation
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GSFC SpaceCube

- Small, light-weight, reconfigurable multi-processor platform for space flight applications demanding extreme processing capabilities
- Based on Xilinx Virtex 4 FX60 FPGAs, 2 per processor card
- Stackable architecture

Flight Box

Mechanical: 7.5-lbs, 5”x5”x7”
Power: 37W (HST Application)
SpaceCube Processor Card

• General: 4”x4” card, Back-to-Back FPGAs (x2), 7W typical power
• Memory: 1GB SDRAM, 1GB Flash, 16KB SRAM, 16KB PROM
• Interfaces: 20 bi-dir differential signals, JTAG
• Backplane: Power, 42 single-ended, 8 LVDM, 2 I2C, POR
SpaceCube Processor Card

Top Side

Bottom Side
Hubble Servicing Mission 4 (STS-125)

• **Relative Navigation Sensors (RNS)** – HST Payload
  – Record images of HST during docking and release, in particular the Soft Capture Mechanism
  – Perform on-orbit position and attitude estimation (Pose)

• **RNS SpaceCube: Main Avionics Box**
  – Controlled 3 cameras, GPS, 960GB memory, telemetry module, shuttle Ku downlink
  – Hosted Linux, VxWorks, C&DH, Automatic Gain and Integration Control, 2 pose image processing algorithms, TMR’d self-configuration scrubber using ICAP
  – Recorded GPS/AGC/POSE flight logs to flash
  – Consisted of 2 processors, 2 low-voltage power cards, 2 digital control cards, 1 JPEG2000 compression card
Relative Navigation Sensors

• RNS originated from HST robotic service mission
• RNS Hardware
  – 3 1024x1024 cameras
  – GPS Navigator
  – SpaceCube
  – Telemetry Module
  – Recorder (8 120GB hard drives)
  – Power Module
  – Ground Terminal
  
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<th>FPGAs</th>
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TOTAL: 28

• RNS operations conducted from JSC Space Shuttle Mission Control Center, Houston TX
RNS Hardware

MULE Carrier

RNS Avionics Panel

MAPLD 2009 - Session A

STS-125 Payload Bay
On Orbit

RNS Cameras

Tough to see, but our cameras and SpaceCube are watching
Xilinx FPGA Design(s)

- Heavy PowerPC usage
- Logic: 62.5-125MHz, Processor: 250MHz
- Used 3 of 4 Xilinxes at 60-80% resource utilization

High-Level Example Xilinx Design (POSE #1 FPGA on Processor Card 1)
Tracking Algorithms on SpaceCube

Flight Image

Hardware Edge Detection

PPC Search for Features
Tracking Algorithms on SpaceCube

Long Range Camera on Rendezvous

- GNFR POSE ESTIMATE
- GMT: 139.16:28:43.757
- Frame ID: 0x73F13002
- Quaternion: 0.7265, -0.67387, 0.03428, 0.12983
- Position (meters): 1.4498, 7.8250, -81.4431
- Pose Quality Confidence: 88.235%

Flight Image

RNS Tracking Solution

Short Range Camera on Deploy

- GNFR POSE ESTIMATE
- GMT: 139.31:37:17.231
- Frame ID: 0x3172418
- Quaternion: -0.64560, 0.27127, 0.65614, -0.27391
- Position (meters): -0.0979, -0.1355, -2.5048
- Pose Quality Confidence: 84.706%

Flight Image

RNS Tracking Solution
RNS Results Summary

- SpaceCube enabled RNS to meet all objectives
  - Recorded 6 hours of camera and GPS data
  - Successfully tracked HST during rendezvous for 21 minutes and deploy for 15 minutes
  - Sent 100,000+ compressed images to ground

- SpaceCube powered for 60 hours (8 in SAA)
  - 2 configuration SEUs in SAA scrubbed out
  - 1 PowerPC SEE that watchdog repaired
HST Tracking

Note: This is the HANDOUT version of this presentation, actual version contains movies

Rendezvous

Deploy
What’s Next?

• Just completed raw imagery downloads at GSFC
• Looking for another flight for RNS hardware
  – Possible ISS flight for robotic demonstration
  – Hubble Robotic De-orbit Mission?
• Flight spare SpaceCube going to ISS (STS-129)
  – Serve as NASA test bed for radiation mitigation
• Building two new versions of SpaceCube
  – Covered in Session E presentation
Questions?

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Acronyms

• FPGA: Field Programmable Gate Array
• I2C: Inter-Integrated Circuit
• ICAP: Internal Configuration Access Port
• ISS: International Space Station
• LVDM: Low Voltage Differential Multi-drop
• MULE: Multi-Use Logistics Equipment
• POR: Power On Reset
• PPC: PowerPC
• SEE: Single Event Effect
• SEU: Single Event Upset
• TMR: Triple Module Redundancy